TEST REPORT

Standard IEC TS 62910:2020

TUV SUD Test Report for Utility-interconnected photovoltaic inverters – Test procedure for Under voltage ride-through measurements

Report No.: Date of issue: Project handler:	64.290.23.31217.01 2023-07-18 Jinjing Peng
Testing laboratory: Address: Testing location:	TÜV SÜD Certification and Testing (China) Co., Ltd. Guangzhou Branch TÜV SÜD Testing Center, D1 building, No. 63 Chuangqi Road, Shilou Town, Panyu District, Guangzhou 511447, China Same as above
Client: Client number: Address: Contact person:	Huawei Technologies Co., Ltd. 041829 Administration Building Headquarters of Huawei Technologies Co., Ltd.Bantian, Longgang District 518129 Shenzhen PEOPLE'S REPUBLIC OF CHINA Wu Shao
Standard:	This TUV SUD test report form is based on the following requirements: IEC TS 62910:2020
TRF number and revision*:*	TRF IEC TS 62910:2020 rev.2/2020-07
TRF originated by:	TUV SUD Product Service, Mr. Billy Qiu
Copyright blank test report:	This test report is based on the content of the standard (see above). The test report considered selected clauses of the a.m. standard(s) and experience gained with product testing. It was prepared by TUV SUD Product Service. TUV SUD Group takes no responsibility for and will not assume liability for damages resulting from the reader's interpretation of the reproduced material due to its placement and context.
General disclaimer:	This test report may only be quoted in full. Any use for advertising purposes must be granted in writing. This report is the result of a single examination of the object in question and is not generally applicable evaluation of the quality of other products in regular production.
Scheme: Non-standard test method: National deviations:	☐ TUV Mark ☐ EU-Directive ☐ without certification ☐ GS Mark ☐ NRTL Mark ☒ Type verification of conformity ☐ No ☒ Yes, see details under Summary of testing N/A
Number of pages *(Report)*: Number of pages *(Attachments)*:	27 N/A
Compiled by:	Jinjing Peng
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Test sample:	Solar Inverter
Type of test object:	Type Test
Trademark:	
Model and/or type reference:	SUN2000-330KTL-H1, SUN2000-330KTL-H2
Rating(s):	See page 4
Manufacturer: Manufacturer number: Address:	Huawei Technologies Co., Ltd. 041829 Administration Building Headquarters of Huawei Technologies Co., Ltd.Bantian, Longgang District 518129 Shenzhen PEOPLE'S REPUBLIC OF CHINA
Sub-contractors/ tests (clause): Name:	N/A N/A
Order description:	☒ Complete test according to TRF ☐ Partial test according to manufacturer's specifications ☐ Preliminary test ☐ Spot check ☐ Others:
Date of order: Date of receipt of test item: Date(s) of performance of test:	2023-07-03 2023-07-05 2023-07-06 to 2023-07-15

Test item particulars:

Clause	Requirement
Cl. 5	Under voltage ride-through

Remark: The model SUN2000-330KTL-H1 was selected as representative testing.

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Summary of testing:

☐ deviation(s) found

☒ no deviations found

If additional information is necessary, please provide

The testing was performed as to manufacturer's specification for under voltage ride-through (UVRT) requirement of standard "Central Electricity Authority (Technical Standards for Connectivity to the Grid) (Amendment) Regulations, 2019". The detail of this specification is duplicated on page 13;

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General product information:

1. The inverter is non-isolated PV inverter for connection with public medium or high voltage grid, for outdoor or indoor use.

2. The adjustable power factor range of SUN2000-330KTL-H1 and SUN2000-330KTL-H2 is 0.8 inductive(under-excited) to 0.8 capacitive(over-excited).

3. LVRT logic is as follow:

Determination of entering LVRT mode: Any phase voltage is lower than 0.9Un, the inverter will enter LVRT mode.

LVRT mode behavior: During LVRT fault, positive and negative sequence of reactive current is determined by k-factor. K-factor of positive sequence is 2 and K-factor of negative sequence is 0. The injection of reactive current is first priority. The supply of active has the second priority and the active power preferably be maintained during voltage drop, unless the rated apparent current is reached. Under unbalance voltage fault, the maximum injection of reactive current is limited to 0.4In.

4. The inverter is designed for fixed mounted on the wall.

5. The firmware version : V500R023. The software version : V500R023C00

Model differences:

SUN2000-330KTL-H1 and SUN2000-330KTL-H2 have same electric circuits topology design, same enclosure structure design, same main control circuits and firmware. The output power and current are limited by software.

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Ratings:

Model:	SUN2000-330KTL-H1	SUN2000-330KTL-H2
PV input parameter		
Maximum input voltage	1500 Vd.c.	
MPPT voltage range	500~1500 Vd.c.	
Maximum input current	6*65 Ad.c.	
PV I_{SC}	6*115 Ad.c.	
Grid parameter		
Rated output voltage	800 Va.c., 3W~ +PE	
Rated output frequency	50 Hz	
Rated output current	216.5 Aa.c.	198.4 Aa.c.
Maximum continuous output current	238.2 Aa.c.	238.2 Aa.c.
Rated output active power	300000 W	275000 W
Maximum continuous output power	330000 W	330000 W
Maximum continuous output apparent power	330000 VA	330000 VA
Power factor	0.8 inductive(under-excited) to 0.8 capacitive(over-excited)	

Attachments: N/A

General remarks:

"(see remark #)" refers to a remark appended to the report.
"(see appended table)" refers to a table appended to the report.
*Throughout this report **a point** is used as the decimal separator.*
The test results presented in this report relate only to the object tested.
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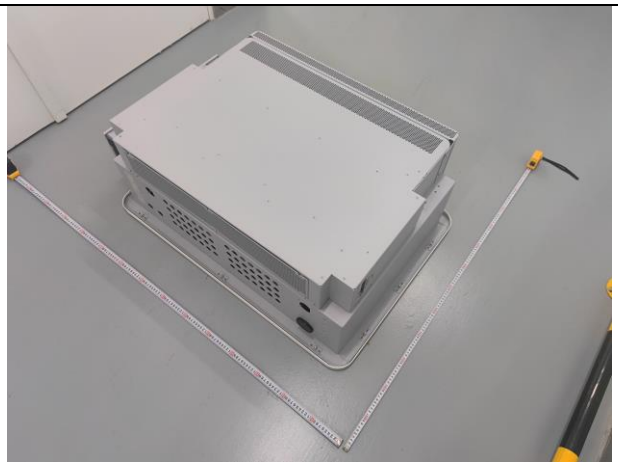
Picture of the product:

Front view



Bottom view

Left side view

Right side view

AC side terminal block

DC side terminal block

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Clause	Requirement + Test	result – Remark	Verdict
4	**Test circuit and equipment**		
4.1	General	Three phase short-circuit fault and Two-phase short-circuit fault and one-phase short-circuit with ground was tested for UVRT.	P
4.2	Test circuit		P
4.3	Test equipment		P
4.3.1	Measuring instruments		P
4.3.2	DC source	The PV array simulator is used	P
4.3.3	Short-circuit emulator	The short-circuit emulator is used	P
4.3.4	Converter based grid simulator		N/A
5	**Test**		
5.1	Test protocol		P
	The UVRT test protocol is designed to verify that the EUT responds appropriately to voltage drops (due to grid faults). During the test, the EUT shall demonstrate that it can:		P
	- Appropriately detect the simulated fault.		P
	- Ride through the event and continue operation as specified in the applicable curves.		P
	- Not suffer any damage from the event.		P
	The response to the voltage drop specified in Table 3 shall be recorded over the EUT operating period with two output power ranges:		P
	a) between 0,1 Pn and 0,3 Pn;	The 0.2 Pn was tested	P
	b) above 0,9 Pn;		P
	and with two fault conditions:		P
	c) three-phase drop;		P
	d) two-phase drop or single-phase drop.	Two-phase with ground	P
	The tests should be carried out at least twice at each test point listed in Table 3.		N/A
5.2	Test curve		P
	The UVRT response characteristic shall meet the requirements of the UVRT curve specified by different countries and regions as needed(see also Annex C).	Meet the requirement of UVRT curve of india CEA	P
5.3	Test procedure		P
5.3.1	Pre-test		P

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Clause	Requirement + Test	result – Remark	Verdict
	Prior to the fault simulation tests, the EUT should run in normal operating mode. The selected UVRT curve should be used to identify voltage drop points, including the lowest point and the inflection point, as well as other random points in the curve. Selection of the drop time should follow the requirement of the applicable country or region.		P
5.3.2	No-load test		P
	Prior to the load test, adjust the fault emulator to simulate symmetrical and asymmetrical voltage drops without EUT connection, and validate that the measured results are as intended. This step ensures that the amplitude of voltage and drop duration can match the requirements in Figure 5.		P
5.3.3	Tolerance		P
	The tolerances for drop depth and duration during the no-load test shall reference the requirement of Figure 6 in IEC 61400-21:2008, and not exceed the values shown in Figure 5.		P
	The tolerance for voltage magnitude is ±5 % of rated voltage for the period before and during the voltage drop. The tolerance for voltage magnitude is ±10 % of rated voltage during the period after voltage is recovered. The tolerances shall be measured between 0 and +5 % of rated voltage for the lowest point and the inflection point under no-load conditions.		P
	The duration of each voltage drop is determined according to the requirements of the applicable UVRT curve. The tolerance range for both drop duration and rise time prefers 40 ms.		P
5.3.4	Load test		P
	Tests under load shall be carried out after the no-load test results successfully meet the performance requirements. The parameters of the grid fault simulator should be consistent with the no-load test.		P
	With the EUT connected to the grid fault simulator device and the PV simulator(or PV array), the output power should be set to (0,1~0,3)Pn and above 0,9Pn separately. Additional load tests at other power levels	The output power is set to 0.2 Pn and 1.0 Pn	P

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Clause	Requirement + Test	result – Remark	Verdict
	should be performed as determined by the specific country or regional requirements.		
	During the UVRT test, MP1, MP2, and MP3 (shown in Figure 1) shall be selected as the test points for measuring and recording the values of voltage and current.	MP3 was selected as the test point	P
	The waveform and data of the measured voltage and current at the measuring points shall be recorded by the data acquisition device from time A prior to the voltage drop to time B after the subsequent voltage rise. For “A” and “B”, specific data should be determined by different countries or regions.	See appended table	P
6	**Assessment criteria**		
	The various assessment criteria is determined by the requirements of the different countries or regions. The characteristics and performance criteria for utilization are shown in Annex B, and can be referenced by a local user.		P
Annex A	**Circuit faults and voltage drops** (informative)		
A.1	Fault types		P
A.2	Voltage drops		P
Annex B	**Determination of critical performance values in UVRT testing** (informative)		
B.1	General	Meet the requirement of india CEA	P
B.2	Drop depth ratio	Meet the requirement of india CEA	P
B.3	Ride-through time	Meet the requirement of india CEA	P
B.4	Reactive current	Meet the requirement of india CEA	P
B.5	Active power	Meet the requirement of india CEA	P
Annex C	**Requirements of the UVRT curve** (informative)		
C.1	General	Meet the requirement of india CEA	P
C.2	UVRT curve	Meet the requirement of india CEA	P
C.3	Test points	Meet the requirement of india CEA	P

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Specification of national requirement

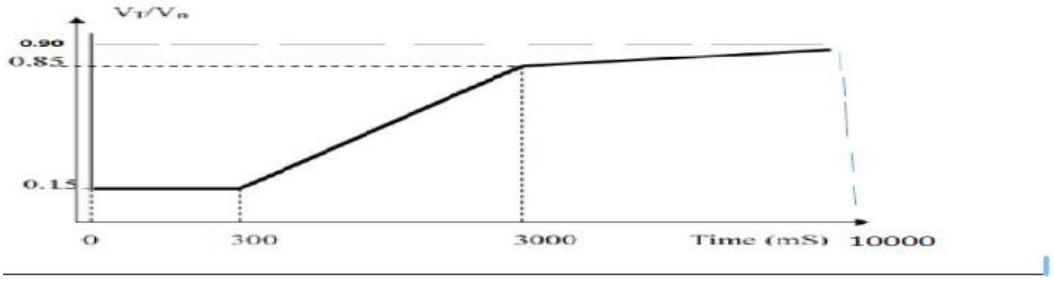
Name of the standard or grid code with clause reference:

Central Electricity Authority (Technical Standards for Connectivity to the Grid) (Amendment) Regulations, 2019.

The generating station connected to the grid, shall remain connected to the grid when voltage at the interconnection point on any or all phases dips up to the level depicted by the thick lines in the following curve:

UVRT curve:

V_T : Actual Voltage; Vn: Nominal Voltage—



Reactive current, active power and recover time requirement:

Provided that during the voltage dip, the supply of reactive power has first priority, while the supply of active power has second priority and the active power preferably be maintained during voltage drops, provided, a reduction in active power within the plant's design specifications is acceptable and active power be restored to at least 90% of the pre-fault level within 1 sec of restoration of voltage.

A typical ∆/Y transformer is assumed between PCC and PV inverter. According to the standard IEC TS 62910 table A.4 & A.5, the voltage amplitude and phase changes are shown below:

Residual voltage of fault phase [p. u.]	Two-phase short-circuit fault with ground					
	Phase A		Phase B		Phase C	
	Am.	Ph.	Am.	Ph.	Am.	Ph.
0.15	1	0	0.5166	165.436	0.5166	194.564
0.25	1	0	0.5449	156.587	0.5449	203.413
0.50	1	0	0.6614	139.107	0.6614	220.893
0.80	1	0	0.8544	125.818	0.8544	234.183
0.85	1	0	0.8899	124.186	0.8899	235.814
0.87	1	0	0.9043	123.569	0.9043	236.431
0.90	1	0	0.9260	122.680	0.9260	237.320
1	1	0	1	120	1	240

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Summary of test condition for UVRT								
Group	Phase fault	EUT output conditions	Dip depth[p.u.]	Fault duration [ms]	Active power	Reactive Power	Test No.	Recover time limit
			Set value	Requirement	Requirement			
1	Three-phase	Full load (100%Pn)	＜0.15Un	350ms	Pn	Maximum	1.1.1 (a)	1s
		Partial load (20%Pn)			20%Pn	Maximum	1.1.2 (a)	
	Two-phase	Full load (100%Pn)	＜0.15Un	350ms	Pn	Maximum	1.2.1 (a)	
		Partial load (20%Pn)			20%Pn	Maximum	1.2.2 (a)	
2	Three-phase	Full load (100%Pn)	0.45-0.5Un	1650ms	Pn	Maximum	2.1.1 (a)	1s
		Partial load (20%Pn)			20%Pn	Maximum	2.1.2 (a)	
	Two-phase	Full load (100%Pn)	0.45-0.5Un	1650ms	Pn	Maximum	2.2.1 (a)	
		Partial load (20%Pn)			20%Pn	Maximum	2.2.2 (a)	
3	Three-phase	Full load (100%Pn)	0.80Un-0.85Un	3500ms	Pn	Maximum	3.1.1 (a)	1s
		Partial load (20%Pn)			20%Pn	Maximum	3.1.2 (a)	
	Two-phase	Full load (100%Pn)	0.80Un-0.85Un	3500ms	Pn	Maximum	3.2.1 (a)	
		Partial load (20%Pn)			20%Pn	Maximum	3.2.2 (a)	
4	Three-phase	Full load (100%Pn)	0.90Un	11000ms	Pn	Maximum	4.1.1 (a)	1s
		Partial load (20%Pn)			20%Pn	Maximum	4.1.2 (a)	
	Two-phase	Full load (100%Pn)	0.90Un	11000ms	Pn	Maximum	4.2.1 (a)	
		Partial load (20%Pn)			20%Pn	Maximum	4.2.2 (a)	

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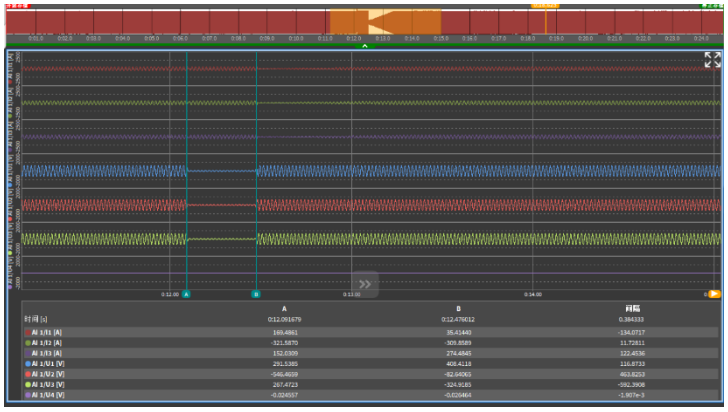
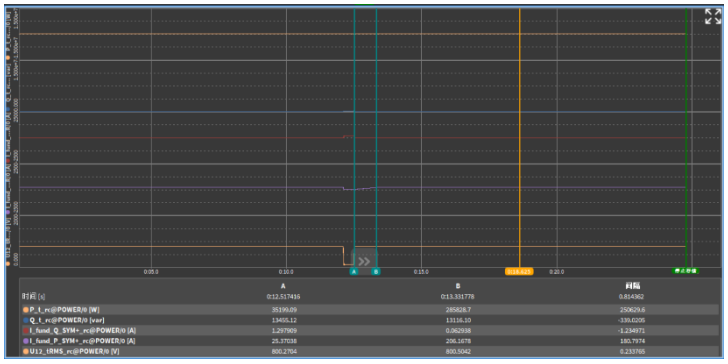
Test Number	1.1.1 (a)					
Requirement						
Phase fault	Three-phase	Power load		Full load (100%Pn)	AC Frequency	50Hz
Dip depth[p.u.] -set value	0.1 Un			Set fault duration [ms]		350
Before fault occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		303291.30
	800.48	800.56	800.50			
Output current (A)	218.64	219.44	218.44	Output reactive power (var)		4778.54
During fault						
Fault Duration (ms)	359.52ms					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		303.22
	86.20	85.74	86.28			
Output current (A)	214.97	216.05	214.62	Output reactive power (var)		31840.90
Output active current (A)	-0.36			Output reactive current (A)		217.25
After occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W, after 1s)		296100.20
	800.49	800.55	800.46			
Output current (A)	213.43	214.40	213.10	Output reactive power (var)		8043.68
Recover time (ms)	814.4			Mean output active power in 5s (W)		60112.98
Graphic during testing						





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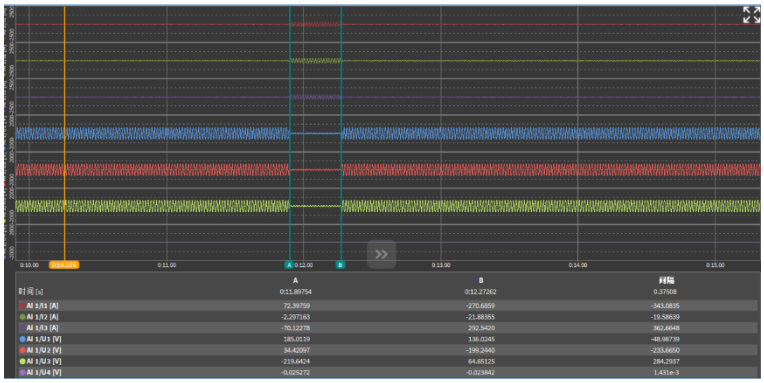
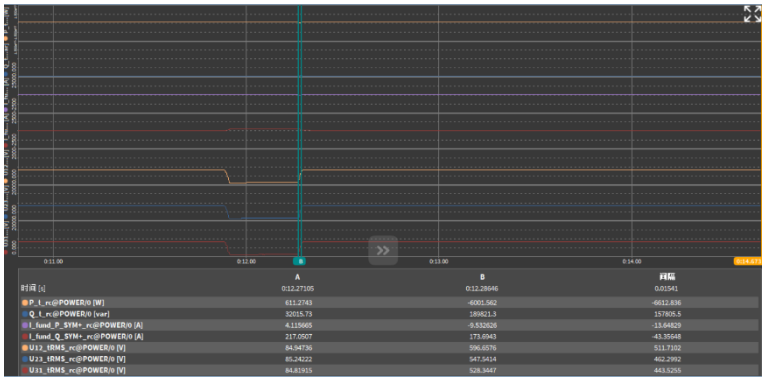
Test Number	1.1.2 (a)					
Requirement						
Phase fault	Three-phase	Power load		Partial load (20%Pn)	AC Frequency	50Hz
Dip depth[p.u.] -set value	0.1 Un			Set fault duration [ms]		350
Before fault occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		59958.66
	799.47	799.72	799.50			
Output current (A)	43.53	43.46	43.31	Output reactive power (var)		4757.83
During fault						
Fault Duration (ms)	352.41					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		604.87
	84.79	85.26	84.95			
Output current (A)	216.28	217.73	216.44	Output reactive power (var)		31901.22
Output active current (A)	3.70			Output reactive current (A)		217.15
After occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W, after 1s)		59965.45
	799.50	799.72	799.50			
Output current (A)	43.70	43.69	43.54	Output reactive power (var)		7535.92
Recover time (ms)	15.4			Mean output active power in 5s (W)		60112.98
Graphic during testing						





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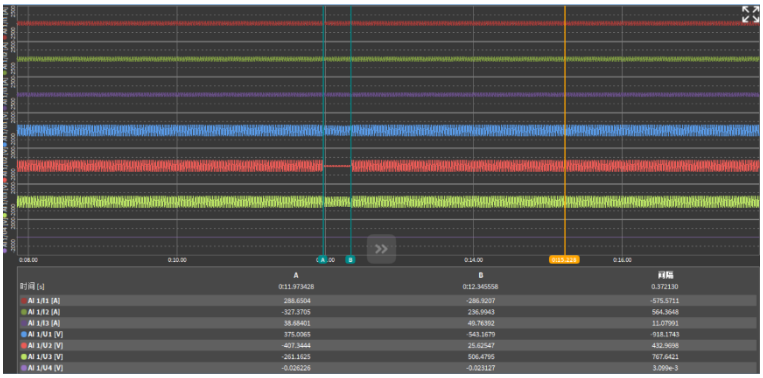
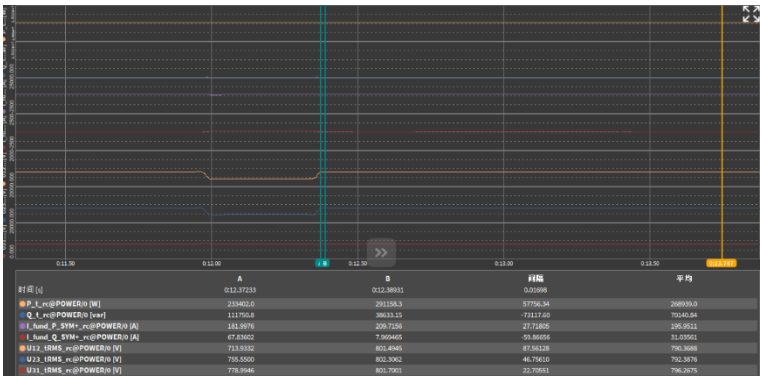
Test Number	1.2.1 (a)					
Requirement						
Phase fault	Two-phase	Power load		Full load (100%Pn)	AC Frequency	50Hz
Dip depth[p.u.] -set value	0.1 Un			Set fault duration [ms]		350
Before fault occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		303261.30
	800.49	800.53	800.46			
Output current (A)	218.61	219.42	218.22	Output reactive power (var)		4738.67
During fault						
Fault Duration (ms)	352.20					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		145092.20
	409.76	410.89	799.13			
Output current (A)	204.45	211.05	211.09	Output reactive power (var)		101812.30
Output active current (A)	187.96			Output reactive current (A)		88.97
After occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W, after 1s)		302954.80
	800.49	800.54	800.46			
Output current (A)	218.43	219.49	218.03	Output reactive power (var)		8588.25
Recover time (ms)	17.0			Mean output active power in 5s (W)		303347.30
Graphic during testing						





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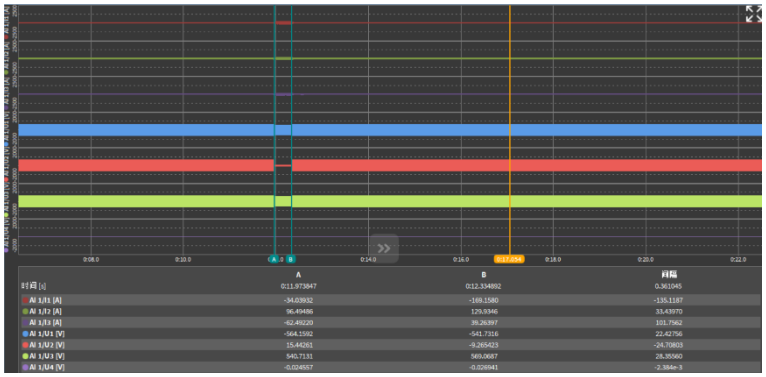
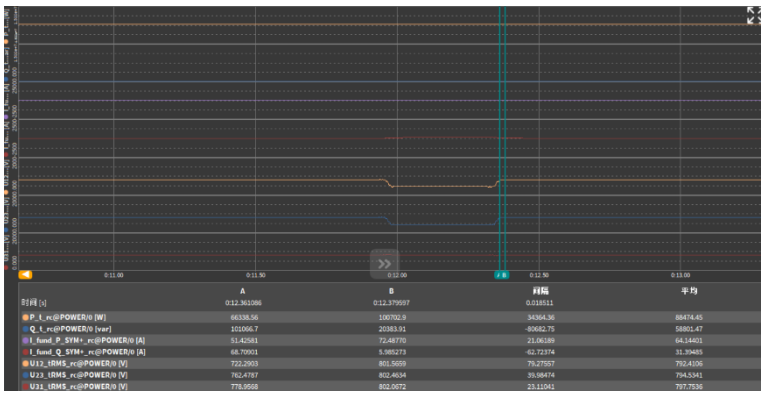
Test Number	1.2.2 (a)					
Requirement						
Phase fault	Two-phase	Power load		Patial load (20%Pn)	AC Frequency	50Hz
Dip depth[p.u.] -set value	0.1 Un			Set fault duration [ms]		350
Before fault occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		60078.54
	799.44	799.72	799.49			
Output current (A)	43.73	43.69	43.53	Output reactive power (var)		6737.83
During fault						
Fault Duration (ms)	359.98					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		42573.08
	413.04	407.07	798.20			
Output current (A)	102.80	107.52	105.70	Output reactive power (var)		77582.14
Output active current (A)	56.93			Output reactive current (A)		86.45
After occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W, after 1s)		59979.45
	799.47	799.70	799.48			
Output current (A)	43.57	43.59	43.35	Output reactive power (var)		5614.52
Recover time (ms)	18.5			Mean output active power in 5s (W)		60161.13
Graphic during testing						





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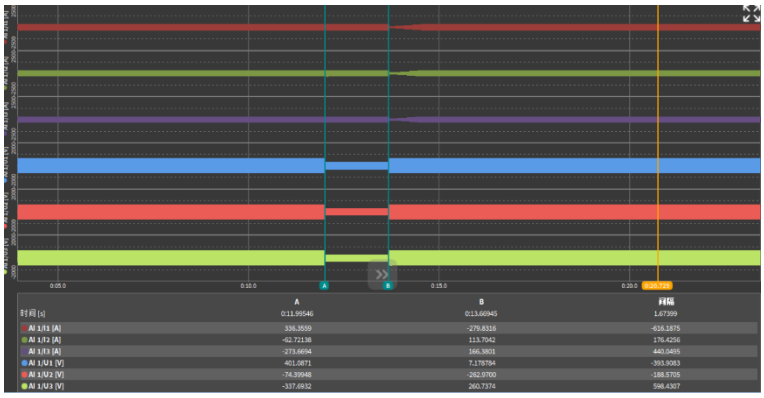
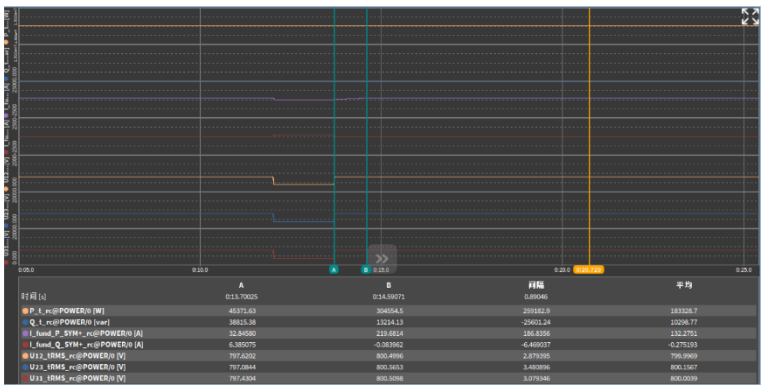
Test Number	2.1.1 (a)					
Requirement						
Phase fault	Three-phase	Power load		Full load (100%Pn)	AC Frequency	50Hz
Dip depth[p.u.] -set value	0.45 Un			Set fault duration [ms]		1650
Before fault occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		303255.40
	800.50	800.55	800.49			
Output current (A)	218.60	219.43	218.19	Output reactive power (var)		4872.01
During fault						
Fault Duration (ms)	1654.38					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		12932.71
	364.86	365.13	364.86			
Output current (A)	219.32	220.17	218.84	Output reactive power (var)		137978.80
Output active current (A)	20.36			Output reactive current (A)		217.58
After occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W, after 1s)		303157.10
	800.49	800.56	809.49			
Output current (A)	218.51	219.52	218.15	Output reactive power (var)		8076.91
Recover time (ms)	890.5			Mean output active power in 5s (W)		281971.80
Graphic during testing						
						
						

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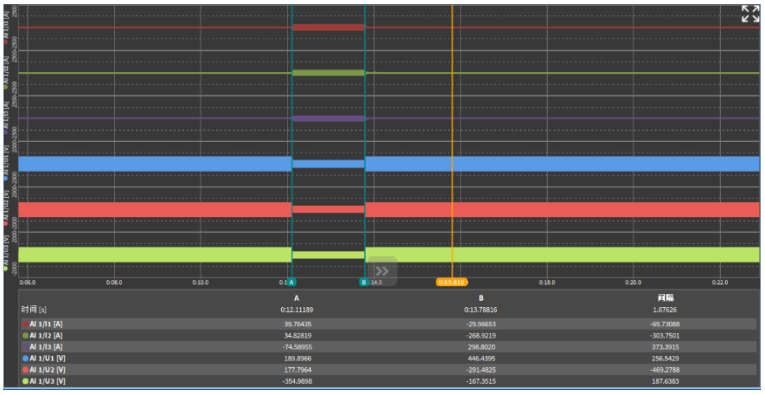
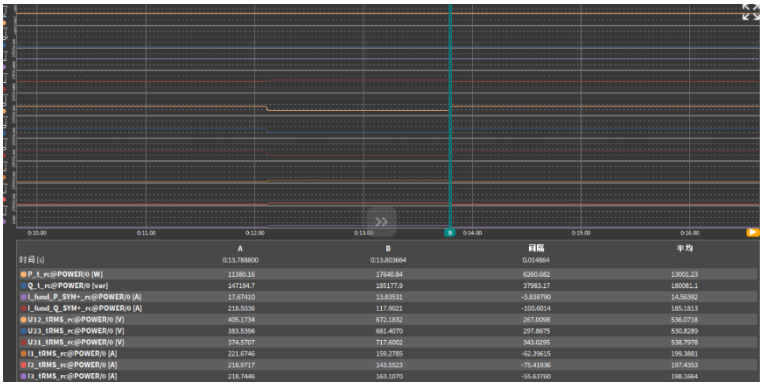
Test Number	2.1.2 (a)					
Requirement						
Phase fault	Three-phase	Power load		Partial load (20%Pn)	AC Frequency	50Hz
Dip depth[p.u.] -set value	0.45 Un			Set fault duration [ms]		1650
Before fault occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		59978.93
	799.45	799.73	799.52			
Output current (A)	43.65	43.62	43.46	Output reactive power (var)		6652.28
During fault						
Fault Duration (ms)	1650.45					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		12618.82
	364.73	365.10	364.71			
Output current (A)	219.24	220.09	218.74	Output reactive power (var)		138044.90
Output active current (A)	19.95			Output reactive current (A)		217.89
After occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W, after 1s)		59921.19
	799.48	799.71	799.49			
Output current (A)	43.65	43.63	43.50	Output reactive power (var)		7268.14
Recover time (ms)	14.9			Mean output active power in 5s (W)		59986.71
Graphic during testing						





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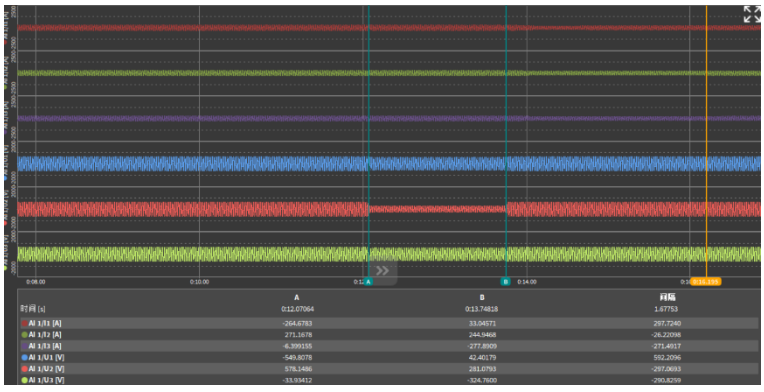
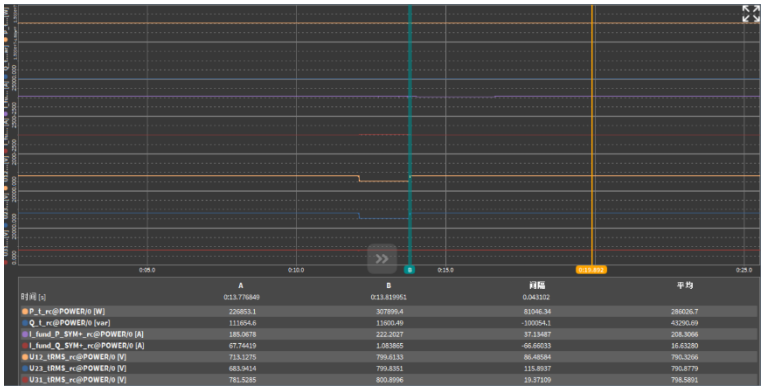
Test Number	2.2.1 (a)					
Requirement						
Phase fault	Two-phase	Power load		Full load (100%Pn)	AC Frequency	50Hz
Dip depth[p.u.] -set value	0.45 Un			Set fault duration [ms]		1650
Before fault occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		303335.00
	800.47	800.49	800.44			
Output current (A)	218.65	219.51	218.26	Output reactive power (var)		4850.37
During fault						
Fault Duration (ms)	1667.56					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		198023.20
	508.91	512.42	802.28			
Output current (A)	215.39	217.11	216.78	Output reactive power (var)		10663.40
Output active current (A)	196.33			Output reactive current (A)		89.60
After occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W, after 1s)		264609.60
	800.30	800.40	800.29			
Output current (A)	190.74	191.66	190.50	Output reactive power (var)		7614.35
Recover time (ms)	43.1			Mean output active power in 5s (W)		255152.90
Graphic during testing						





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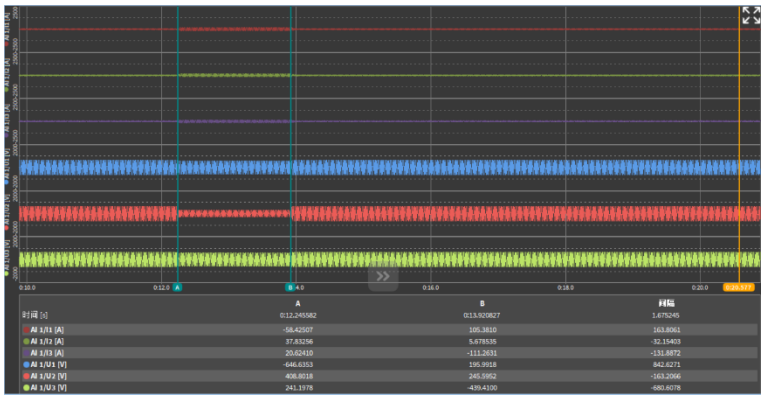
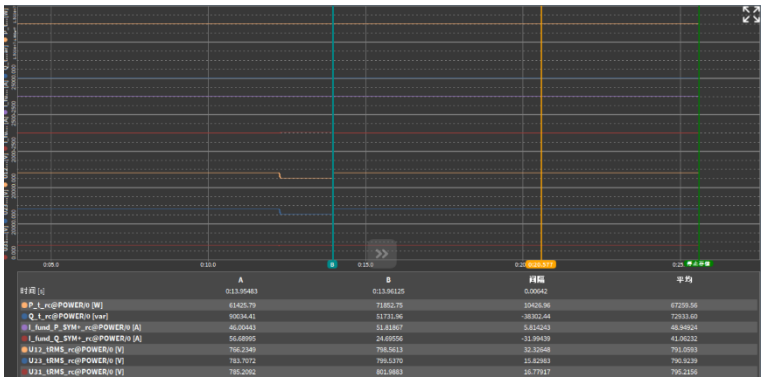
Test Number	2.2.2 (a)					
Requirement						
Phase fault	Two-phase	Power load		Partial load (20%Pn)	AC Frequency	50Hz
Dip depth[p.u.] -set value	0.45 Un			Set fault duration [ms]		1650
Before fault occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		59968.34
	799.40	799.65	799.40			
Output current (A)	43.55	43.45	43.34	Output reactive power (var)		4817.97
During fault						
Fault Duration (ms)	1664.88					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		60118.89
	509.63	509.35	801.56			
Output current (A)	108.28	107.00	108.36	Output reactive power (var)		94661.37
Output active current (A)	59.55			Output reactive current (A)		89.18
After occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W, after 1s)		59925.58
	799.40	799.65	799.42			
Output current (A)	43.67	43.65	43.50	Output reactive power (var)		7367.44
Recover time (ms)	6.4			Mean output active power in 5s (W)		59966.25
Graphic during testing						





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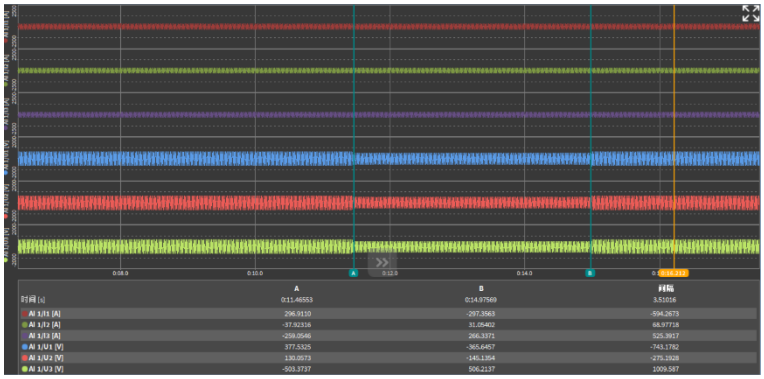
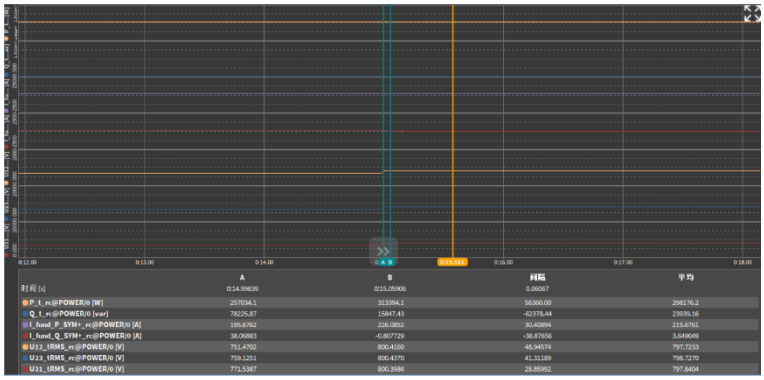
Test Number	3.1.1 (a)					
Requirement						
Phase fault	Three-phase	Power load		Full load (100%Pn)	AC Frequency	50Hz
Dip depth[p.u.] -set value	0.80 Un			Set fault duration [ms]		3500
Before fault occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		303250.90
	800.49	800.56	800.48			
Output current (A)	218.60	219.41	218.19	Output reactive power (var)		4667.95
During fault						
Fault Duration (ms)	3515.50					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		228174.20
	642.52	642.60	642.49			
Output current (A)	222.04	222.97	221.34	Output reactive power (var)		95100.48
Output active current (A)	205.03			Output reactive current (A)		84.80
After occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W, after 1s)		303101.90
	800.51	800.57	800.48			
Output current (A)	218.45	219.47	218.12	Output reactive power (var)		7800.41
Recover time (ms)	60.7			Mean output active power in 5s (W)		303273.50
Graphic during testing						





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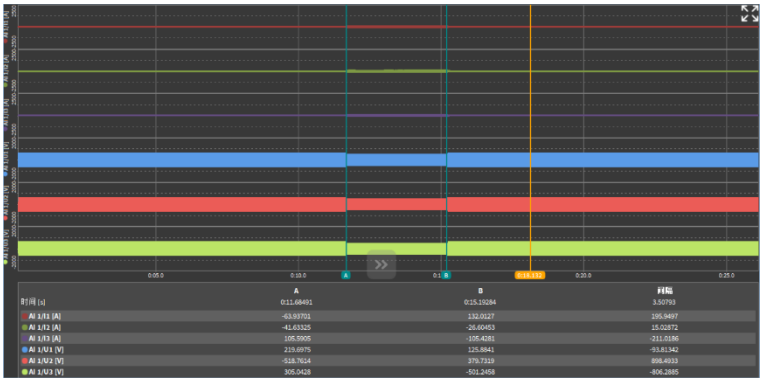
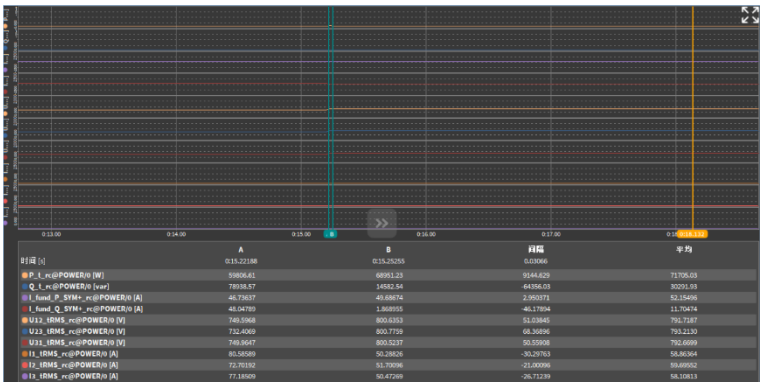
Test Number	3.1.2 (a)					
Requirement						
Phase fault	Three-phase	Power load		Partial load (20%Pn)	AC Frequency	50Hz
Dip depth[p.u.] -set value	0.80 Un			Set fault duration [ms]		3500
Before fault occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		59953.54
	799.47	799.72	799.50			
Output current (A)	43.54	43.46	43.30	Output reactive power (var)		4876.67
During fault						
Fault Duration (ms)	3514.47					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		60199.31
	641.54	641.83	641.60			
Output current (A)	100.40	100.83	100.20	Output reactive power (var)		94050.89
Output active current (A)	54.17			Output reactive current (A)		84.45
After occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W, after 1s)		59853.43
	799.46	799.72	799.50			
Output current (A)	43.60	43.59	43.45	Output reactive power (var)		73433.99
Recover time (ms)	30.7			Mean output active power in 5s (W)		59964.95
Graphic during testing						





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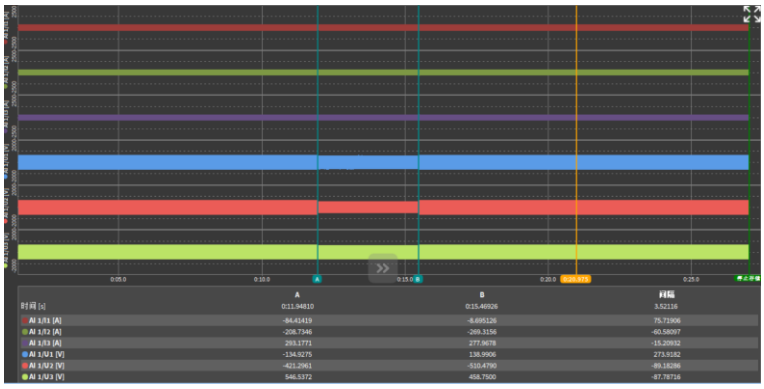
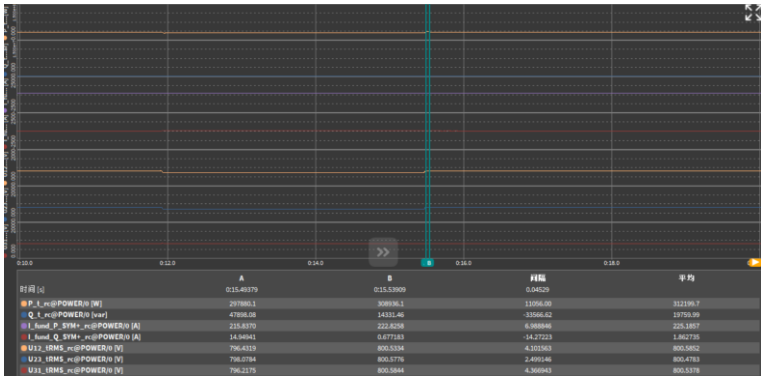
Test Number	3.2.1 (a)					
Requirement						
Phase fault	Two-phase	Power load		Full load (100%Pn)	AC Frequency	50Hz
Dip depth[p.u.] -set value	0.80 Un			Set fault duration [ms]		3500
Before fault occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		303280.50
	800.46	800.49	800.41			
Output current (A)	218.65	219.47	218.20	Output reactive power (var)		4821.69
During fault						
Fault Duration (ms)	3516.53					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		269388.10
	684.60	685.90	801.10			
Output current (A)	219.38	222.81	219.58	Output reactive power (var)		61488.83
Output active current (A)	215.85			Output reactive current (A)		42.06
After occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W, after 1s)		303057.40
	800.43	800.51	800.44			
Output current (A)	218.43	219.46	218.09	Output reactive power (var)		7843.37
Recover time (ms)	45.3			Mean output active power in 5s (W)		303084.20
Graphic during testing						





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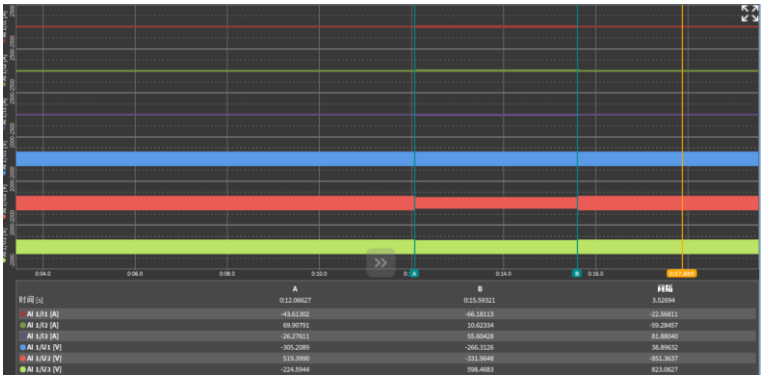
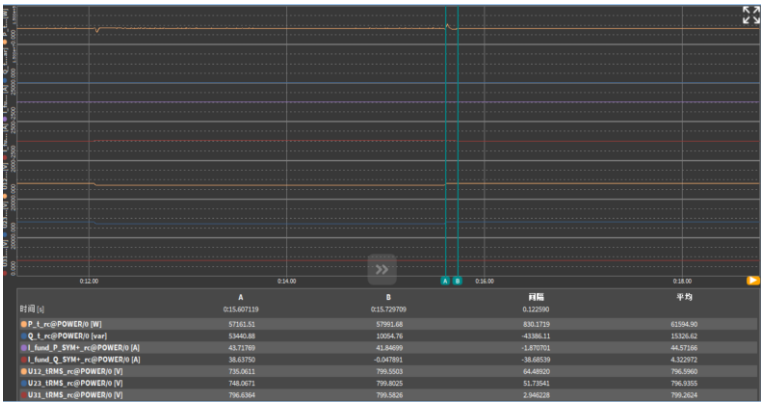
Test Number	3.2.2 (a)					
Requirement						
Phase fault	Two-phase	Power load		Partial load (20%Pn)	AC Frequency	50Hz
Dip depth[p.u.] -set value	0.80 Un			Set fault duration [ms]		3500
Before fault occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		60004.53
	799.40	799.65	799.40			
Output current (A)	43.68	43.66	43.47	Output reactive power (var)		6718.70
During fault						
Fault Duration (ms)	3533.38					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		60118.91
	684.30	684.41	800.24			
Output current (A)	64.26	64.88	65.03	Output reactive power (var)		54272.38
Output active current (A)	48.24			Output reactive current (A)		42.19
After occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W, after 1s)		59857.27
	799.40	799.65	799.41			
Output current (A)	43.61	43.62	43.46	Output reactive power (var)		7415.50
Recover time (ms)	122.6			Mean output active power in 5s (W)		59932.91
Graphic during testing						





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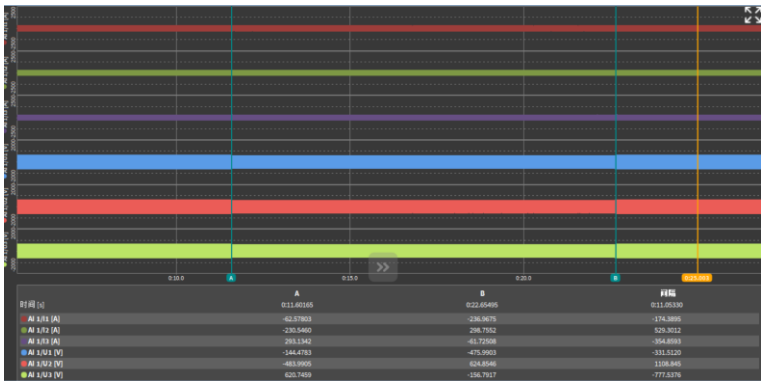
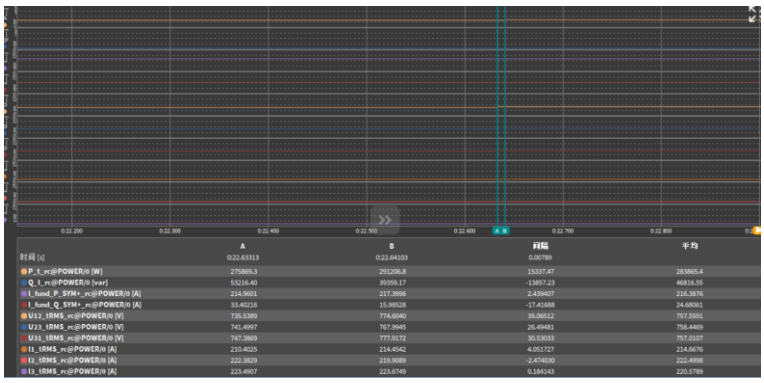
Test Number	4.1.1 (a)					
Requirement						
Phase fault	Three-phase	Power load		Full load (100%Pn)	AC Frequency	50Hz
Dip depth[p.u.] -set value	0.90 Un			Set fault duration [ms]		11000
Before fault occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		303274.80
	800.47	800.55	800.49			
Output current (A)	218.62	219.43	218.20	Output reactive power (var)		4663.13
During fault						
Fault Duration (ms)	11049					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		268785.40
	721.69	721.82	721.74			
Output current (A)	219.53	220.66	219.11	Output reactive power (var)		56832.25
Output active current (A)	215.05			Output reactive current (A)		42.34
After occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W, after 1s)		303021.40
	800.49	800.56	800.48			
Output current (A)	218.41	219.42	218.05	Output reactive power (var)		7938.54
Recover time (ms)	7.9			Mean output active power in 5s (W)		303039.00
Graphic during testing						





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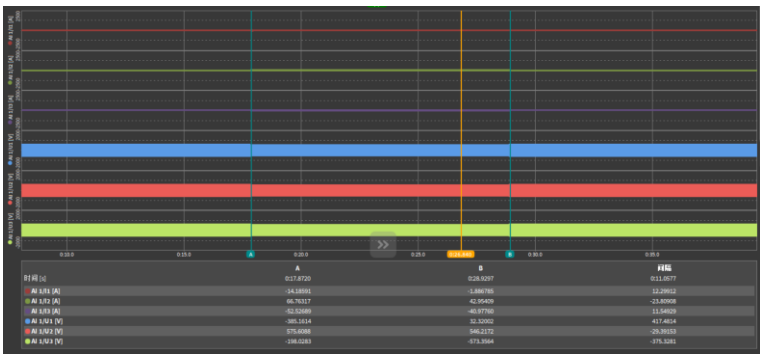
Test Number	4.1.2 (a)				
Requirement					
Phase fault	Three-phase	Power load	Partial load (20%Pn)	AC Frequency	50Hz
Dip depth[p.u.] -set value	0.90 Un		Set fault duration [ms]		11000
Before fault occurs					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)	60034.43
	799.46	799.72	799.49		
Output current (A)	43.69	43.65	43.49	Output reactive power (var)	6667.83
During fault					
Fault Duration (ms)	11018				
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)	60173.40
	720.54	720.81	720.59		
Output current (A)	64.61	64.80	64.41	Output reactive power (var)	53666.71
Output active current (A)	48.21			Output reactive current (A)	42.14
After occurs					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W, after 1s)	59750.52
	799.47	799.72	799.50		
Output current (A)	43.52	43.52	43.34	Output reactive power (var)	7230.51
Recover time (ms)	206.9			Mean output active power in 5s (W)	59801.28
Graphic during testing					



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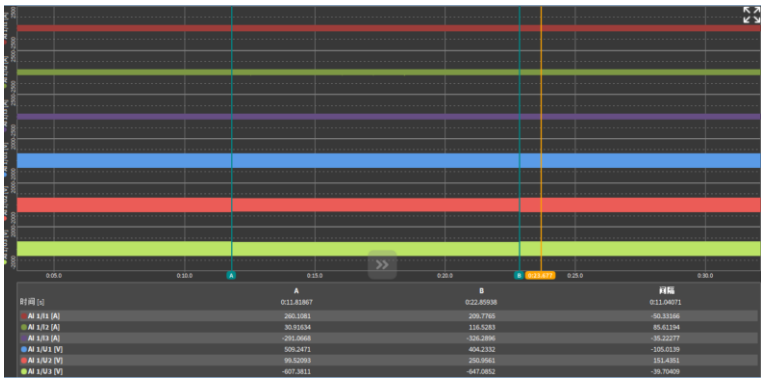
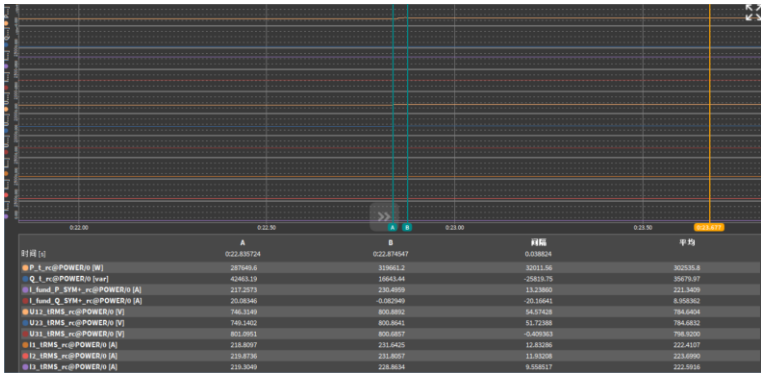
Test Number	4.2.1 (a)					
Requirement						
Phase fault	Two-phase	Power load		Full load (100%Pn)	AC Frequency	50Hz
Dip depth[p.u.] -set value	0.90 Un			Set fault duration [ms]		11000
Before fault occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		303251.40
	800.44	800.50	800.44			
Output current (A)	218.60	219.44	218.21	Output reactive power (var)		4801.07
During fault						
Fault Duration (ms)	11035.83					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)		43580.03
	741.78	742.43	800.54			
Output current (A)	219.28	221.23	219.28	Output reactive power (var)		43580.03
Output active current (A)	217.71			Output reactive current (A)		20.95
After occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W, after 1s)		303074.00
	800.46	800.51	800.43			
Output current (A)	218.44	219.47	218.11	Output reactive power (var)		8007.89
Recover time (ms)	38.8			Mean output active power in 5s (W)		303121.60
Graphic during testing						





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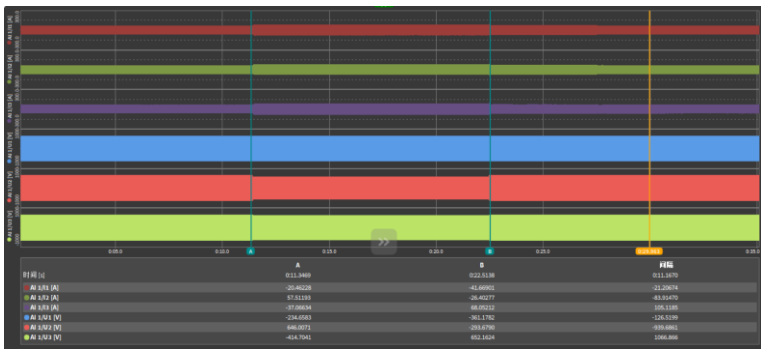
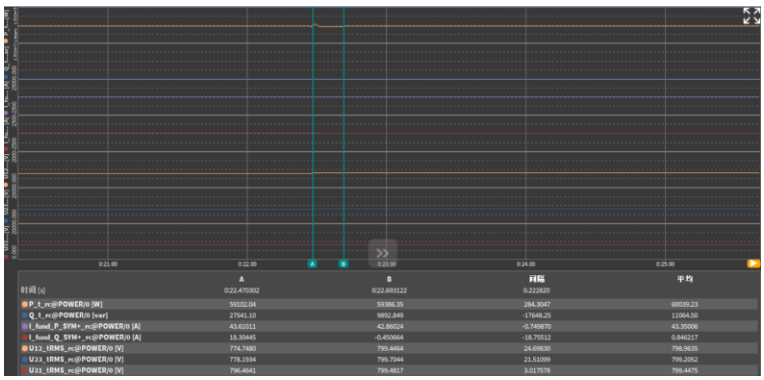
Test Number	4.2.2 (a)					
Requirement						
Phase fault	Two-phase	Power load	Partial load (20%Pn)	AC Frequency	50Hz	
Dip depth[p.u.] -set value	0.90 Un		Set fault duration [ms]	11000		
Before fault occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)	59951.37	
	799.42	799.66	799.45			
Output current (A)	43.52	43.45	43.32	Output reactive power (var)	4731.39	
During fault						
Fault Duration (ms)	11167.00					
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W)	60004.15	
	741.12	741.33	799.55			
Output current (A)	50.27	50.69	50.38	Output reactive power (var)	28560.53	
Output active current (A)	45.59			Output reactive current (A)	20.64	
After occurs						
Output voltage (V)	L1-L2	L2-L3	L3-L1	Output active power (W, after 1s)	59729.16	
	799.42	799.67	799.42			
Output current (A)	43.52	43.52	43.35	Output reactive power (var)	7357.92	
Recover time (ms)	222.8			Mean output active power in 5s (W)	59729.35	
Graphic during testing						
						
						

--- End of test report---

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