

Certificado de la funcionalidad LVRT y HVTR PARQUE FOTOVOLTAICO CARACOLI

W a man		K.	Fan					G	. River	а		M. Yu		
CanadianSolar	C	OLLAB	ORA	TORS			VERIFIED BY VALIDAT				IDATED	BY		
Engineering	Engineering													
&	GROUP	TYPE	cou	INTRY			PROJECT	CODE			PROGRESSI	VE	REV	ISION
Construction	CAR	М	С	О	2	7	4	5	1	0	5	7	0	0
CLASSIFICATION: FOR VALIDATION UTILIZATION SCOPE: FOR CONSTRUCTION														

REV	DESCRIPCIÓN	ELABORADOR	REVISOR	APROBADOR	FECHA
00	Sent for Revision	K. Fan	G. Rivera	M. Yu	21/09/2022

CANADIAN SOLAR VALIDATION							
-	J. Ventura	R. Duran					
COLABORADOR	VERIFICADOR	VALIDADOR					



TEST REPORT IEC TS 62910

Utility-interconnected photovoltaic inverters - Test procedure for low voltage ride-through measurements

Report

Total number of pages 81

Testing Laboratory...... DEKRA Testing and Certification (Suzhou) Co., Ltd.

P.R. China

Applicant's name...... Sungrow Power Supply Co., Ltd.

Development Zone, 230088, Hefei, P. R. China

Test specification:

Standard: IEC TS 62910:2020

Non-standard test method.....: N/A

Test Report Form No..... IEC TS 62910_V2.0

Test Report Form(s) Originator: DEKRA Testing and Certification (Suzhou) Co., Ltd.

Master TRF Dated 2020-08

Test item description Grid-connected PV inverter

Manufacturer Sungrow Power Supply Co., Ltd.

No.1699 Xiyou Rd., New & High Technology Industrial

Development Zone, 230088, Hefei, P. R. China

Model/Type reference SG3125HV-30, SG3125HV-31, SG3125HV-32

Page 2 of 81 Report No.: 6092407.51

Operating temperature range: - 35°C to + 60°C Ratings....: Protective class: I Ingress protection rating: IP65 (Optional IP55) Power factor range (adjustable): 0.8 leading...0.8 lagging SG3125HV-30: PV input: Max. 1500 Vdc, MPPT voltage range: 875-1300 Vdc, max current: 3997 A, Isc PV: 10000 A Output: 600V, 3~, 50/60 Hz, max 3308 A, rated 3125 kW, max 3437 kVA SG3125HV-31: PV input: Max. 1500 Vdc, MPPT voltage range: 915-1300 Vdc, max current: 3997 A, Isc PV: 10000 A Output: 630V, 3~, 50/60 Hz, max 3308 A, rated 3125 kW, max 3610 kVA SG3125HV-32: PV input: Max. 1500 Vdc, MPPT voltage range: 960-1300 Vdc,

max current: 3997 A, Isc PV: 10000 A

3781 kVA

Output: 660V, 3~, 50/60 Hz, max 3308 A, rated 3125 kW, max

Page 3 of 81 Report No.: 6092407.51

Responsible Testing Laboratory (as applicable)	, testing procedure and t	esting location(s):		
☐ Testing Laboratory:	DEKRA Testing and Certification (Suzhou) Co., Ltd.			
Testing location/ address:	No.99, Hongye Road, S Jiangsu, P.R. China	Suzhou Industrial Park, Suzhou,		
Associated Testing Laboratory:	Shanghai Testing & Ispe Equipment Co.,Ltd	ection Institute for Electrical		
Testing location/ address	No.505, Wuning Road,	Putuo District,Shanghai, China		
Tested by (name, function, signature):	Albert Liang	Albert lions Jasanlero		
Approved by (name, function, signature):	Jason Guo	Saenlin		
Testing procedure: CTF Stage 1:				
Testing location/ address:				
Tested by (name, function, signature):				
Approved by (name, function, signature):				
Testing procedure: CTF Stage 2:				
Testing location/ address:				
Tested by (name + signature):				
Witnessed by (name, function, signature):				
Approved by (name, function, signature):				
Testing procedure: CTF Stage 3:				
Testing procedure: CTF Stage 4:				
Testing location/ address:				
Tested by (name, function, signature):				
Witnessed by (name, function, signature):				
Approved by (name, function, signature):				
Supervised by (name, function, signature):				

Page 4 of 81 Report No.: 6092407.51

Rating label:







Page 5 of 81 Report No.: 6092407.51

Warning Label:



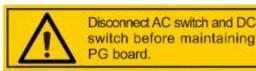


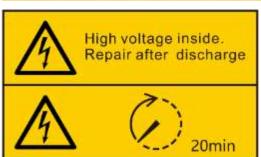


















Page 6 of 81 Report No.: 6092407.51

Test item particulars:					
Equipment mobility:	movable <u>fixed</u>	hand-h transpo		statior for bu	nary ilding-in
Connection to the mains:	pluggable ed permanent d			direct plu	
Enviromental category:	<u>outdoor</u>		indoor unconditic	onal	indoor conditional
Over voltage category Mains	OVC I	OVC II	OVC	<u>III</u>	OVC IV
Over voltage category PV	OVC I	OVC II	OVC	III	OVC IV
Mains supply tolerance (%)	±10%				
Tested for power systems	TN				
IT testing, phase-phase voltage (V)	N/A				
Class of equipment	<u>Class I</u> Not classifie	Class d	II	Class III	
Mass of equipment (kg)	3200				
Pollution degree	Outside PD3	3; Inside P	D2		
IP protection class	IP65 (Option	ıal IP55)			
Possible test case verdicts:					
- test case does not apply to the test object	N/A				
- test object does meet the requirement	P (Pass)				
- test object does not meet the requirement	F (Fail)				
- this clause is information reference for installation:	Info.				
Testing:					
Date of receipt of test item	2020-10-25	(samples p	orovided b	y applica	ant)
Date (s) of performance of tests	2020-10-25	to 2020-11	-30		
General remarks:					
The test results presented in this report relate only to the object tested. This report shall not be reproduced, except in full, without the written approval of the Issuing testing laboratory. The measurement result is considered in conformance with the requirement if it is within the prescribed limit, It is not necessary to account the uncertainty associated with the measurement result. This report is only for reference and is not used for legal proof function in China market. The information provided by the customer in this report may affect the validity of the results, the test lab is not responsible for it.					
"(See Enclosure #)" refers to additional information ap "(see appended table)" refers to a table appended to the		ereport.			
Throughout this report a ☐ comma / ☒ point is used	as the decima	al separato	or.		

Page 7 of 81 Report No.: 6092407.51

Name and address of factory (ies)

1. Sungrow Power Supply Co., Ltd.

No.1699 Xiyou Rd., New & High Technology Industrial Development Zone,

Hefei 230088 P.R. China

2. Sungrow Power Supply Co., Ltd.

No. 608 Changning Avenue, New & High Technology Industrial Development Zone,

Hefei 230088 P.R. China

3. Sungrow Developers (India) Private Limited

No. 85, Kaniminike village, Kengeri hobli Bangalore South Taluk,

560074 Bangalore, India

Page 8 of 81 Report No.: 6092407.51

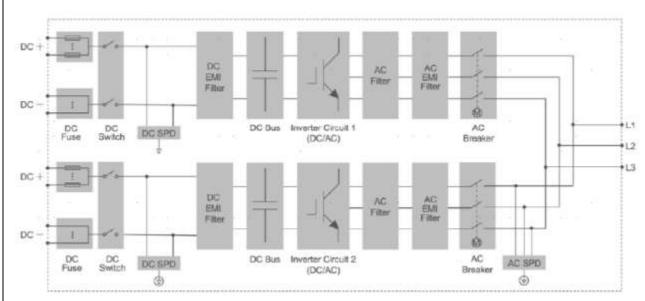
General product information:

Brief description:

The PCE under test (EUT) is Grid-Connected PV Inverter which utilizes the advanced power electronics conversion components such as MosFET, IGBT, IPM to convert the variable DC power generated from the photovoltaic (PV) arrays to the stable utility AC power which can be fed into the commercial electrical grid.

The PCE under test is three-phase Grid-Connected PV Inverter for solar power generation with the rated output power of 3125 kW. The external circuit breakers or fuses for PV array and Grid connection are required which the statements are provided in the installation manual.

Block Diagram:



The models SG3125HV-31, SG3125HV-30 are identical to SG3125HV-32 except for the model name and electrical ratings.

Unless otherwise specified, all the tests were conducted on the basic model of SG3125HV-32 to represent the others.

The product was tested on:

Firmware version:

DSP_SG3125HV-30_V1_A

LCD SG3125HV-30 V1 A

Unless otherwise specified, all tests were conducted on basic model of SG3125HV-32 to represent the other models.

Page 9 of 81 Report No.: 6092407.51

	IEC TS 62910	Report No., oue	2107.01
Clause	Requirement - Test	Result - Remark	Verdict
4	Test circuit and equipment		Р
4.1	General		Р
	The circuits and equipment described in this clause are developed to allow tests that simulate the full range of anticipated grid faults, including:		Р
	Single phase to ground fault (any phase)		Р
	Two phase isolated fault, between any two phases		Р
	Two phase grounded fault, involving any two phases		Р
	Three phase short-circuit fault.		Р
	A full discussion of these faults and the resulting impact on voltage magnitude and phase angles is included in Annex A.		Р
	The short circuit emulator and grid simulator described in 4.3.3 and 4.3.4 are informative examples and are not intended to restrict design flexibility. Other designs may be used to achieve equivalent test functionality.	The grid simulator used to achieve test of 4.3.4.	Р
4.2	Test circuit		Р
	The LVRT test circuit includes a DC source, the EUT, a grid fault simulator and the grid. A PV simulator (or PV array) provides input energy for the EUT. The output of the EUT is connected to the grid via a grid fault simulator, as shown in Figure 1.	PV array simulator and the grid simulator used in the LVRT test circuit.	Р
	U _{Grid} Simulator Transformer (optional)		
	NOTE MP1 is the measurement point between the grid and the grid fault simulator; MP2 is the measurement point at the high voltage side of the transformer; MP3 is the measurement point at the low voltage side of the transformer. Figure 1 – Testing circuit diagram		
4.3	Test equipment		Р
4.3.1	Measuring instruments		Р
	Waveforms shall be measured by a device with memory function, for example, a storage or digital oscilloscope, or a high speed data acquisition device. Accuracy of the oscilloscope or data acquisition system should be at least 0.2% of full scale. The analogue to A/D of the measurement device shall have at least 12 bit resolution (in order to maintain the required measurement accuracy).		Р

		Page 10 of 81	Report No.: 609	2407.51
		IEC TS 62910	T	_
Clause	Requirement - Test		Result - Remark	Verdict
	Voltage transducers (or voltage transducers (or current transfo sensors for measurement. The should be 0.5 % of full scale or select the transducer measurin normal value of the signal to be measuring range shall not exceed value of the measured signal. Traple 1 – Accuracy of the measured signal to be the measured signal.	rmers) are the required accuracy of the transducers better. It is necessary to g range depending on the emeasured. The selected eed 150 % of the normal The transducer accuracy ble 1		Р
	Measurement device	Accuracy		
	Data acquisition device	0,2 % full scale		
	Voltage transducer	0,5 % full scale		
	Current transducer	0,5 % full scale		
4.3.2	DC source		Р	
	A PV array, PV array simulator with PV characteristics may be source to supply input energy f EUT input source, the DC power of supplying the EUT maximum power levels during the test, at input operating voltages of the	PV array simulator used as the DC power source to supply input energy.	P	
	The PV simulator should emula characteristic of the PV module EUT is designed. The response should not be longer than the N of EUT.		Р	
	For a EUT under test without g the DC side and AC side, the o shall not be earthed.		Р	
	The equivalent capacitance be simulator and earth should be a to minimize the impact on the E		Р	
	A PV array used as the EUT in of matching the EUT input pow test conditions. It is necessary which the solar irradiance is stamore than 5 % during the test.		Р	
4.3.3	Short-circuit emulator		The grid simulator used to achieve LVRT function.	N/A

Page 11 of 81

Report No.: 6092407.51

IEC TS 62910							
Clause	Requirement - Test	Result - Remark	Verdict				
	As part of the grid simulator device, the short-circuit emulator is used to create the voltage drops due to short-circuits between the two or three phases, or between one or two phases to ground, via the impedance network Z ₁ and Z ₂ as shown in the test device layout in Figure 2. Back to back circuit (optional) S ₁ S ₂ (optional) Figure 2 – Short-circuit emulator		N/A				
	The impedance Z_1 is used to limit the effect of the short circuit on the utility service that powers the test circuit. The sizing of Z_1 shall therefore account for all test sequences to be performed and limit the short-circuit current taken from the grid to values that do not cause an excessive reduction of the grid voltage. Considering an acceptable voltage reduction of at most 5 % when performing the test, the minimum value of Z_1 shall be at least $20 \times Z_{\text{Grid}}$, where Z_{Grid} is the grid short-circuit impedance measured at the test circuit connection point.		N/A				
	To ensure that the test is realistic, however, the apparent short-circuit power (S_{EUT}) available at the EUT connection node N_{EUT} should be at least equal to $3\times Pn$. where Pn is the rated power of the EUT (minimum value $S_{\text{EUT}} > 3\times Pn$. recommended $S_{\text{EUT}} = 5$ to $6\times Pn$), This means that during the short-circuit tests, the contribution of current through Z_1 and Z_2 from the grid remains dominant compared to the current contributed by the EUT. In this way, the inverter current does not create a significant voltage rise for the duration of the test relative to the no-load drop.		N/A				
	The two conditions described above define the minimum and maximum limits of Z_1 . The two conditions combined also define the limit criteria for the choice of a grid infrastructure suitable for performing the test with the impedance circuit. If the grid infrastructure cannot meet the above requirements, an alternative test circuit utilizing a back-to-back converter is allowed, as shown in Figure 2 and may be added to reduce the grid short-circuit impedance Z_{Grid} .		N/A				

Page 12 of 81

Report No.: 6092407.51

			IEC	TS 62910)		
Clause	Requirement - Te	st				Result - Remark	Verdict
	Generally, the X/F circuit emulator m impedance values also appropriate t should be charact in order to reprodifound in HV as we	ay close to s for differe hat the ind terised by a uce the typ	the trans nt countrie uctive imp an X/R rati ical minim	mission line es and regi edances Z io equal to num values	e ons. It is 1 and Z ₂ at least 3,		N/A
	A bypass connect prevent overheati the execution of e	ng of the ir	npedance				N/A
	The voltage drop Z ₂ by the switch S created twice in a parallel switch S ₂ ' Z ₂ +Z _{Grid}) shall be magnitudes. For emagnitude is 50 % (Z ₁ +Z ₂ +Z _{Grid}) shou	5 ₂ ' If the volume short period is normally adjusted to example, was of the rate.	tage drop od (for dou y used. The the requir hen the re ed voltage	is required able drop te se value of red voltage equired volt	to be ests), a Z ₂ /(Z ₁ + c tage		N/A
	The switch S ₂ shabetween connectiphase, two-phase switch S ₂ cannot switch S ₁ may be used to select who switches may be power electronic of	on and dis or three-poe indeper used to chether the fa either mec	connection hase tests dently cor oose the f ault is to e	n of Z ₂ for s s. If the pha ntrolled, the ault phase arth or not.	single ase of e serial . S ₂ is All		N/A
	The status of swit performing the test to fault types is shadown	st The statu	us of switc				N/A
	The test report sh and Z ₂ ' the related used. In addition, the voltage level a documented.	d X/R ratio, the grid sh	and a des	scription of power avai	the circuit ilable at		N/A
	The status of swit 2.	ches and f		N/A			
	Fault type	Di-		status	-		
	Phase A to ground	Phase A of B ₁ Closed	Phase B of B ₁ Open	Phase C of B ₁ Open	B ₂ Closed		
	Phase B to ground	Open	Closed	Open	Closed		
	Phase C to ground Phase A and B to ground	Open	Open	Closed	Closed		
	Phase B and C to ground	Open	Closed	Closed	Closed		
	Phase C and A to ground	Closed	Open	Closed	Closed		
	Phase A and B Phase B and C	Closed	Closed	Open Closed	Open Open		
	Phase C and A	Closed	Open	Closed	Open		
	Phase A, B and C	Closed	Closed	Closed		1	
	The state of the s	81 32 00000	3700 In				
	During the period of voltage druinterval between the above two	S_1 should be ope actions shall be very	ned first. S ₂ should short.	be closed after S ₁ is	opened. The time		
	During the period of voltage dri interval between the above two During the period of voltage re time interval between the above	actions shall be very covery, S ₂ should be	short. opened first. S, sh				
1.3.4	During the period of voltage re	actions shall be very covery, S ₂ should be	short. opened first. S, sh				

	Page 13 of 81	Report No.: 609	2407.51
	IEC TS 62910	I	T
Clause	Requirement - Test	Result - Remark	Verdict
	The test circuit mentioned in 4.3.3 is recommended for simulation of grid faults. However, if the test conditions cannot be met, an alternative test circuit utilizing a back-to-back converter is allowed, as shown in Figure 3.		Р
	The test circuit essentially comprises a voltage source with a low internal resistance combined with broadband amplifiers (linear or forced switching type) capable of faithfully reproducing three sinusoidal voltages with controlled harmonic content, and adjustable amplitude, fundamental frequency and phase relationship within broad margins.		Р
	When the converter is used, it shall meet the following requirements:		Р
	 a) It shall be capable of independently controlling the three phases in terms of amplitude and phase angle. b) It shall incorporate impedances ZA, ZS and ZC, that can be adjusted in order to reproduce the ohmic and inductive components of short-circuit impedances that are typical of the grid. c) It shall be capable of reproducing the phase voltages and relative phase angles that occur on the LV side of transformers in the event of each of the various fault types. (See Annex A for the vector representations for each fault). 		Р
	If the programmable voltage source is a bi-directional, controlled capable of replicating the influence of short-circuit impedances Z _A , Z _B , Z _C may be omitted.		Р
5	Test		Р
5.1	Test protocol		Р
	The LVRT test protocol is designed to verify that the EUT responds appropriately to voltage drops (due to grid faults). During the test, the EUT shall demonstrate that it can: • Appropriately detect the simulated fault. • Ride through the event and continue operation as specified in the applicable curves. • Not suffer any damage from the event.		Р

Page 14 of 81 Report No.: 6092407.51 IEC TS 62910 Clause Requirement - Test Result - Remark Verdict The response to the voltage drop specified operating Ρ period with two output power ranges a) between 0.1 Pn and 0.3 Pn; b) above 0.9 P_n; and with two fault conditions: c) three-phase drop; d) two-phase drop or single-phase drop. The tests should be carried out at least twice at each test point listed in Table 3. Table 3 – Test specification for LVRT (indicative) (1 of 2) Drop times Drop depth^b EUT output conditions^d Drop phase^c Full load (above 0,9 Pa) Three-phase Part load (0.1 P. and 0.3 P.) Full load (above 0,9 P_) Part load (0,1 P_n and 0,3 P_n) Full load (above 0,9 P_n) Two-phase to ground Part load (0,1 P_n and 0,3 P_n) Full load (above 0,9 Pn) Single-phase to ground Part load (0,1 P, and 0,3 P,) Single drop Full load (above 0,9 Pg) Three-phase Part load (0,1 $P_{\rm n}$ and 0,3 $P_{\rm n}$) Full load (above 0,9 Pp) Two-phase Part load (0,1 $P_{\rm n}$ and 0,3 $P_{\rm n}$) Full load (above 0,9 Pg) Two-phase to ground Part load (0,1 P_n and 0,3 P_n) Full load (above 0,9 Pn) Single-phase to ground Part load (0,1 P, and 0,3 P,) Table 3 (2 of 2) Drop depthb **Drop times** Drop phase EUT output conditions Full load (above 0.9 P) Part load (0,1 P_n and 0,3 P_n) Full load (above 0,9 P_n) Two-phase Part load $(0,1 P_n \text{ and } 0,3 P_n)$ Full load (above 0,9 P_n) Two-phase to ground Part load (0,1 P_n and 0,3 P_n) Full load (above 0,9 P_n) Single-phase to ground Part load (0,1 P_n and 0,3 P_n) Full load (above 0,9 P_n) Three-phase Part load (0,1 P, and 0,3 P,) Full load (above 0.9 P_) Two-phase Part load (0,1 P_n and 0,3 P_n) Full load (above 0,9 Pa) Two-phase to ground Part load (0,1 P_n and 0,3 P_n) Full load (above 0,9 P_n) Single-phase to ground Part load (0,1 Pn and 0,3 Pn a. Double drop test may be required in some countries or regions. For devices under test not being required for double drop test, above testing points can be omitted. b. Drop depth is the residual voltage during the LVRT testing period which can be decided according 10 the requirement specified by different countries or regions (See Clause B.2 for drop depth ratio calculation.) c. Drop phase can be decided according 10 the requirement specified by different countries or regions; the value of two-phase voltage should be line voltage. d. The test should be carried out under specified K-factor provided by local manufacture 5.2 Test curve Ρ

Page 15 of 81

Report No.: 6092407.51

	IEC TS 62910	. 1000.1.10.1	0032407.31			
Clause	Requirement - Test	Verdict				
	The LVRT response characteristic shall meet the requirements of the LVRT curve specified by different countries and regions as needed. An example LVRT curve is shown in Figure 4. 1,1		P			
	The example curve shows that the EUT should keep operating during operating conditions indicated in the area above the LVRT curve. Specifically, the EUT should keep operating for (t_1-t_0) seconds without disconnecting from the grid when the interconnection voltage drops to 0 % of rated voltage; for (t_2-t_0) seconds when the voltage drops to 30 % of rated voltage; and for (t_3-t_0) seconds when the voltage drops to 70 % of rated voltage. The EUT should disconnect from the grid during operating conditions indicated within the shaded areas.		Р			
	The example shows two types of points on the LVRT curve: the lowest point and the inflection point. Tests shall be carried out at both types of points.		Р			
5.3	Test procedure		Р			
5.3.1	Pre-test		Р			
	Prior to the fault simulation tests. the EUT should run in normal operating mode. The selected LVRT curve should be used to identify voltage drop points. including the lowest point and the inflection point. as well as other random points in the curve. Selection of the drop time should follow the requirement of the applicable country or region.		Р			
5.3.2	No-load test		Р			
	Prior to the load test, adjust the fault emulator to simulate symmetrical and asymmetrical voltage drops without EUT connection. and validate that the measured results are as intended. This step ensures that the amplitude of voltage and drop duration can match the requirements in Figure 5.					
5.3.3	Tolerance		Р			
	The tolerances for drop depth and duration during the no- load test shall reference the requirement of Figure 6 in IEC 61400-21 :2008, and not exceed the values shown in Figure 5		Р			

Page 16 of 81

Report No.: 6092407.51

IEC TS 62910						
Clause	Requirement - Test	Result - Remark	Verdict			
	The tolerance for voltage magnitude is ±5% of rated voltage for the period before and during the voltage drop. The tolerance for voltage magnitude is ±10 % of rated voltage during the period after voltage is recovered. The tolerances shall be measured between 0 and +5 % of rated voltage for the lowest point and the inflection point under no-load conditions.		P			
	The duration of each voltage drop is determined according to the requirements of the applicable LVRT curve. The tolerance range for both drop duration and rise time prefers 40ms. ### Time(s) ### Figure 5 – Tolerance of voltage drop		P			
5.3.4	Load test		Р			
	Tests under load shall be carried out after the no-load test results successfully meet the performance requirements. The parameters of the grid fault simulator should be consistent with the no-load test.		Р			
	With the EUT connected to the grid fault simulator device and the PV simulator (or PV array), the output power should be set to $(0.1\text{-}0.3)P_n$ and above $0.9P_n$ separately. Additional load tests at other power levels should be performed as determined by the specific regional requirements.		Р			
	During the LVRT test, MP1, MP2, and MP3 (shown in Figure 1) shall be selected as the test points for measuring and recording the values of voltage and current.		Р			
	The waveform and data of the measured voltage and current at the measuring points shall be recorded by the data acquisition device from time A prior to the voltage drop to time B after the subsequent voltage rise. For "A" and "B", specific data should be determined by different countries or regions.		Р			
6	Assessment criteria		Р			

	Page 17 of 81	Report No.: 6092407.51		
	IEC TS 62910			
Clause	Requirement - Test	Result - Remark	Verdict	
	The various assessment criteria is determined by the requirements of the different countries or regions. The characteristics and performance criteria for utilization are shown in Annex B, and can be referenced by a local user.		Р	

			Page 18 IEC TS 6		Report No.:	6092407.51
Clause	Requireme	ent - Test	Result - Remark	Verdict		
Annex A	Circuit fault	ts and voltage	drops (informative)		Р
A.1	Fault types			P		
	commonly single-phas			ission line are		Р
	two-phase	grounded fault	, and			
	The most o	e short circuit factories to short common one is bunting for over				
		I types of fault	ault phases, the s are shown in Tabl	e A.1.		Р
	Type No.	Short circuit type	Equivalent diagram	Mathematical formulae		
	,	Single-phase (A) short circuit grounded fault	10 21 V0 10 10 10 10 10 10 10 10 10 10 10 10 10	Y_{c_0} =0 I_{c_0} ≠0 I_{c_0} =0		
	2	Single-phase (B) short circuit grounded fault		$V_{\infty}=0$ $I_{t_0}\neq 0$ $I_{t_0}=I_{t_0}=0$		
	9	Single-phase (C) abort circuit grounded fault		$I_{i_0}=0$ $I_{i_0}\neq 0$ $I_{i_0}=I_{i_0}=0$		
	4	Two-phase (AB) short circuit isolated fault	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$V_{i_0} = V_{i_0} = 0$ $I_{i_0} = 0$ $I_{i_0} = 1$		
	6	Two-phase (BC) short circuit isolated fault	Fee $z_1 - z_2 - z_3 - z_4 - z_5 - z_$	$\begin{split} V_{t_0} = & V_{t_0} \neq 0 \\ & I_{t_0} = 0 \\ & I_{t_0} + I_{t_0} = 0 \end{split}$		
	6	Two-phase (CA) short circuit isolated fault	$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c} P_{t_0} \! = \! V_{t_0} \! \neq \! 0 \\ I_{t_0} \! = \! 0 \\ I_{t_0} \! + \! I_{t_0} \! = \! 0 \end{array}$		
	7	Two-phase (AB) short circuit grounded fault	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c} V_{\gamma_2} \! = \! V_{\gamma_2} \! = \! 0 \\ I_{t_0} \! = \! 0 \\ I_{t_0} \! + \! I_{t_0} \! \neq \! 0 \end{array}$		

		ort No.: 6092407.51
Clause	Requirement - Test Result - Remarks	ark Verdict
	8 Two-phase (BC) short circuit grounded tault $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Р
	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	
	Three-phase short- $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	
	NOTE 1 Y_{th} Y_{th} and Y_{th} mean fault voltage of phase A, phase B and phase C at fault point separately. NOTE 2 J_{th} , J_{th} and J_{th} mean fault current of phase A, phase B and phase C at fault point separately. NOTE 3 Type No. 1, 2, 3, 7, 8 and 9 are not applicable for IT system.	
A.2 A .2.1	Voltage drops General	P P
	When a fault occurs, the voltage amplitude in the faulted phase should be decreased. When a fault occurs between two phases, the phase angle should be changed on inverter output side. Due to the different types of line-transformer connections, the magnitude and phase of inverter AC voltage will vary. Figure A.1 shows the circuit topology under the fault condition.	P
	PCC T PV inverter	
	Figure A.1 – Grid fault diagram As indicated in Table A.1, the value of fault phase voltage at the fault point is zero. (If the grid fault type is two-phase short circuit fault without ground, the line voltage between two fault phases should be zero.) Because PCC is the common connection point of the infinite grid, Z _i between the fault point and PCC could be treated as infinite. The voltage drop amplitude and phase deviation in PV inverter AC side have been determined by the value of Z _p and type of transformer.	

Page	20	of	81
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	Page 20 of 81	Report No.: 6092407.51		
	IEC TS 62910	T		
Clause	Requirement - Test	Result - Remark	Verdict	
	The transformer "T" represents the voltage and phase transformation being equivalent to all the transformers between the fault point and the PV inverter, because one or more transformers are connected. The equivalent transformer "T" has only two types -Y/Y or Y/ Δ . In order to simplify the analysis, the transformer windings could be considered as one of two types, Yn/Yn12 and Δ /Yn11, with a ratio of 1.		P	
A.2.2	Three-phase short-circuit fault		Р	
	Figure A.2 - Diagram of voltage vector for three-phase short-circuit fault occurs: Figure A.2 - Diagram of voltage vector for three-phase short-circuit fault Figure A.2(a) shows the angle and phase state with a Yn/Yn12 transformer connection. Figure A.2(b) shows the angle and phase state with a Δ/Yn11 transformer connection. The corresponding relationship between the fault phase and the other two phases is shown in the following Table A.2. Table A.2 - Amplitude and phase changes in three-phase short-circuit fault Residual Voltage of fault		P	
A .2.3	Two-phase short-circuit fault with ground		Р	
	There are three possible two-phase short-circuit earth faults, depending on the fault phases. Taking the two-phase (BC) short circuit fault with ground for example, the change in inverter AC voltage amplitudes and phases are shown below: Jua		P	

Page 21 of 81 Report No.: 6092407.51 IEC TS 62910 Result - Remark Verdict Clause Requirement - Test Figure A.3(a) shows the angle and phase state with a Р Yn/Yn12 transformer connection. Figure A.3(b) shows the angle and phase state with a Δ/Yn11 transformer connection. The corresponding relationship between the fault phase and the other two phases is shown in the following Table A.3. Table A.3 – Amplitude and phase changes in two-phase (BC) short-circuit fault with ground Residual voltage of fault phase With the Yn/Yn12 transformer Phase A Phase B Phase C Phase A Phase B Phase C Am. Ph. Am. % Am. Ph. Ph. Am. Ph. Am. Ph. Ph. Am. 100 0 1 0 1 0 1 30 1 30 30 50 0 0,5 0 0,5 0 0,76 19 0,5 30 0,76 41 0,2 0,2 0,64 0,2 0,64 1 0 0 - 0 - 0,58 0 0 - 0,58 60 NOTE Am. means amplitude and Ph. means the initial phase. A .2.4 Ρ Two-phase short-circuit fault without ground There are three possible two-phase short-circuit earth Ρ faults, depending on the fault phases. Taking the twophase (BC) short circuit fault for example, the change in inverter AC voltage amplitudes and phases are shown below: Ub' Figure A.4 - Diagram of voltage vector of two-phase (BC) short-circuit fault Figure A.4(a) shows the angle and phase state with a Ρ Yn/Yn12 transformer connection. Figure A.4(b) shows the angle and phase state with a Δ /Yn11 transformer connection. The corresponding relationship between the fault phase and the other two phases is shown in the following Table A.4. Table A.4 - Amplitude and phase changes in two-phase (BC) short-circuit fault With the Yn/Yn12 transformer Residual With the ∆/Yn11 transformer voltage of fault phase Phase A Phase B Phase C Phase A Phase B Am. Ph. Am. Ph. Am. Ph. Am. Ph. Am. Ph. 0 1 0 1 0 0,66 19 0,66 0 1 1 30 30 30 100 50 16 0.5 30 44 20 0 0,53 41 0,53 -41 0,87 7 0,2 30 0.87 53 0 0,5 60 0,5 -60 0,866 0 0,866 60 NOTE Am. means amplitude and Ph. means the initial phase A .2.5 Single-phase short-circuit fault with ground Ρ

Page 22 of 81 Report No.: 6092407.51 IEC TS 62910 Clause Requirement - Test Result - Remark Verdict There are three possible single-phase short-circuit faults to Ρ ground, depending on the fault phases. Taking the singlephase A) short circuit fault for example, the change in inverter AC voltage amplitudes and phases are shown below: Figure A.5 – Diagram of voltage vector of single-phase (A) short-circuit fault with ground Figure A.5(a) shows the angle and phase state with a Р Yn/Yn12 transformer connection. Figure A.5(b) shows the angle and phase state with a Δ /Yn11 transformer connection. The corresponding relationship between the fault phase and the other two phases is shown in the following Table A.5. Table A.5 – Amplitude and phase changes in single-phase (A) short-circuit fault with ground Residual voltage of fault phase With the Yn/Yn12 transformer With the Δ/Yn11 transformer Phase A Phase B Phase C Phase A Phase B Phase C Am. Ph. % Am. Ph. Ph. Am. Ph. Ph. 100 0 30 30 30 41 0,5 30 19 0,64 51 0,2 30 1 0 1 0 1 0 0,58 60 0 NOTE Am. means amplitude and Ph. means the initial phase.

Page 23 of 81 Report No.: 6092407.51

	IEC TS 62910	Report No., ous	, <u> </u>
Clause	Requirement - Test	Result - Remark	Verdict
Annex B	Determination of critical performance values in LVRT testing (informative)		P
B.1	General		Р
	This Annex provides suggested methods for determining several of the critical performance values in LVRT testing. Different countries and regions may choose alternate methods according to the requirements of their standards.		Р
B.2	Drop depth ratio.		Р
	As the voltage of the test circuit may deviate from the nominal voltage of system, the rated voltage of the EUT should be used as the reference voltage for calculations of the voltage drop depth ratio, as shown in Formula B.1. As such it is not recommended to use the value of the actual voltage measured prior to the drop test to calculate drop depth.		P
	$A_{\rm n} = \frac{U_{\rm dip}}{U_{\rm n}} \qquad \qquad \text{(B.1)}$ where $A_{\rm n} \text{is the residual voltage ratio;}$ $U_{\rm dip} \text{is the actual voltage during the drop test;}$		
8.3	Un is the rated AC voltage of EUT. Ride-through time		P
	Over the voltage drop period, the EUT shall meet the ride through time requirements corresponding with the applicable voltage drop depths. These requirements will differ depending on countries and regions, however, the LVRT performance should meet or exceed the most demanding requirements for the specified region. LVRT functions tested successfully according to specific ride through requirements should only be applied in corresponding countries and regions where those requirements are applicable.		P
B.4	Reactive current	As require by applicant, reactive current is not requirement over the duration of the voltage drop.	N/A
	If the EUT generates reactive current as a function of voltage drop depth over the duration of the voltage drop, the incremental voltage changes in the un-fault phases caused by the increased reactive current shall not exceed any values specified by the most demanding requirements of the different countries or regions.		N/A

Page 24 of 81 Report No.: 6092407.51

it is required that the reactive output current of the EUT hould change dynamically according to the voltage hange during the drop period, the time period for stimating the value of reactive current should be selected etween the beginning of the voltage drop and the eginning of the voltage recovery. This is shown as the me between t ₁ and t ₂ in Figure B.1. In general, time period etween t ₂ and t ₃ is not over 20 ms. RMS Figure B.1 – Determination of reactive current output	Result - Remark	Verdict N/A
hould change dynamically according to the voltage hange during the drop period, the time period for stimating the value of reactive current should be selected etween the beginning of the voltage drop and the eginning of the voltage recovery. This is shown as the me between t ₁ and t ₂ in Figure B.1. In general, time period etween t ₂ and t ₃ is not over 20 ms.		N/A
U to to to the text of the tex		
he output of reactive current may fluctuate during test. his fluctuation may result in reactive current values that re higher or lower than the standard requirement during he test, especially during the voltage drop period. herefore, the reactive current value measurement should be averaged over the whole drop period.		
ctive power		Р
active power control characteristics are required by the ocal standard during LVRT events, it is necessary to haracterize active powers (p_0) before, during (p_1) and after o_{2} the voltage drop, as shown in Figure B.2.		Р
ctive power (p_1) may fluctuate during the voltage drop sterval, especially at point (p_s) where system voltage ecovery begins. It is therefore misleading to use the value of active power recorded at p_s for active power control essessment. It is suggested instead that an average value of active power be determined over the time between t_1 and t_2 to assess the characteristics of active power ecovery		P
and an analysis of the second	active power control characteristics are required by the al standard during LVRT events, it is necessary to aracterize active powers (p_0) before, during (p_1) and after the voltage drop, as shown in Figure B.2. The power (p_1) may fluctuate during the voltage drop erval, especially at point (p_s) where system voltage covery begins. It is therefore misleading to use the value active power recorded at p_s for active power control sessment. It is suggested instead that an average value active power be determined over the time between t_1 dt t_2 to assess the characteristics of active power covery. RMS PW PD PD PD PD PD PD PD PD PD	active power control characteristics are required by the all standard during LVRT events, it is necessary to arracterize active powers (p_0) before, during (p_1) and after the voltage drop, as shown in Figure B.2. The power (p_1) may fluctuate during the voltage drop erval, especially at point (p_s) where system voltage covery begins. It is therefore misleading to use the value active power recorded at p_s for active power control sessment. It is suggested instead that an average value active power be determined over the time between t_1 dt t_2 to assess the characteristics of active power sovery The power of the powe

5.3.1 Pre-test (Grid simulator setting)									Р
Figure	Fault	ault Fault Duration		L1	L2		L3		Dec mu
rigure	Depth	(ms)	pu	Degree	pu	Degree	pu	Degree	- Pos.pu
	5%	250	0.05	0	0.05	240	0.05	120	0.050
A.2.2	20%	770	0.20	0	0.20	240	0.20	120	0.200
(b)	50%	1800	0.50	0	0.50	240	0.50	120	0.500
	85%	3000	0.85	0	0.85	240	0.85	120	0.850
	5%	250	0.05	0	0.59	268	0.59	92	0.366
A.2.3 (b)	20%	770	0.20	0	0.64	261	0.64	99	0.467
	50%	1800	0.50	0	0.76	251	0.76	109	0.666
	85%	3000	0.85	0	0.93	243	0.93	117	0.900
	5%	250	0.05	0	0.87	268	0.87	92	0.521
A.2.4	20%	770	0.20	0	0.87	263	0.87	97	0.600
(b)	50%	1800	0.50	0	0.90	254	0.90	106	0.750
	85%	3000	0.85	0	0.97	244	0.97	116	0.925
	5%	250	1.00	0	0.59	212	0.59	148	0.683
A.2.5	20%	770	1.00	0	0.64	218	0.64	142	0.733
(b)`	50%	1800	1.00	0	0.76	229	0.76	131	0.833
	85%	3000	1.00	0	0.92	237	0.92	123	0.950

Note:

Δ/Yn11 transformer connection shows the angle and phase state of A.2.2(b), A.2.3(b), A.2.4(b), A.2.5(b).

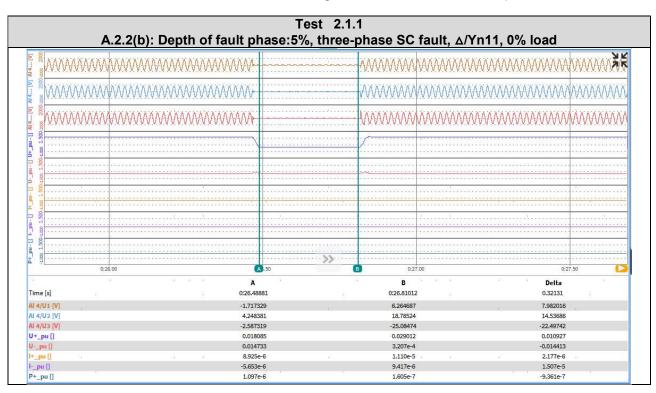
SC: short circuit

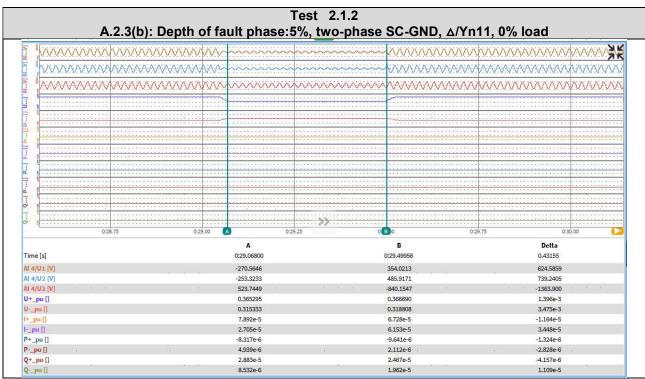
SC-GND: short circuit with ground SC(no ground): short circuit without ground

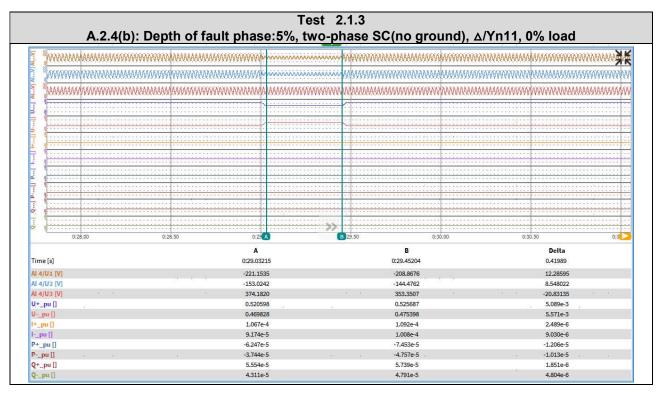
5.3.2(b)	B.2(b) No load Test (△/Yn11 transformer)						
Model: S	G3125HV-32						
Test	Voltage	age Fault turns Measured Fault duration [ms]		Verdict			
1651	Depth [pu]	Fault type	voltage. Pos [pu]	Drop	Maintain	Restore	Verdict
2.1.1		A.2.2 (b)	0.048	16.1	321	19.0	Р
2.1.2	0.05	A.2.3 (b)	0.365	19.8	431	17.5	Р
2.1.3	0.05	A.2.4 (b)	0.520	16.0	419	19.7	Р
2.1.4		A.2.5 (b)	0.677	18.4	415	19.7	Р
2.2.1		A.2.2 (b)	0.211	19.6	870	16.8	Р
2.2.2	0.00	A.2.3 (b)	0.460	14.7	961	18.3	Р
2.2.3	0.20	A.2.4 (b)	0.593	18.2	962	15.9	Р
2.2.4		A.2.5 (b)	0.722	18.2	950	18.2	Р
2.3.1		A.2.2 (b)	0.500	13.2	1930	27.5	Р
2.3.2	0.50	A.2.3 (b)	0.658	13.2	1920	17.5	Р
2.3.3	0.50	A.2.4 (b)	0.745	19.3	1890	19.2	Р
2.3.4		A.2.5 (b)	0.829	14.0	1860	17.5	Р
2.4.1		A.2.2 (b)	0.850	14.9	3110	14.9	Р
2.4.2	0.05	A.2.3 (b)	0.899	14.0	3103	14.1	Р
2.4.3	0.85	A.2.4 (b)	0.925	16.1	3082	14.1	Р
2.4.4		A.2.5 (b)	0.947	16.7	3085	16.7	Р

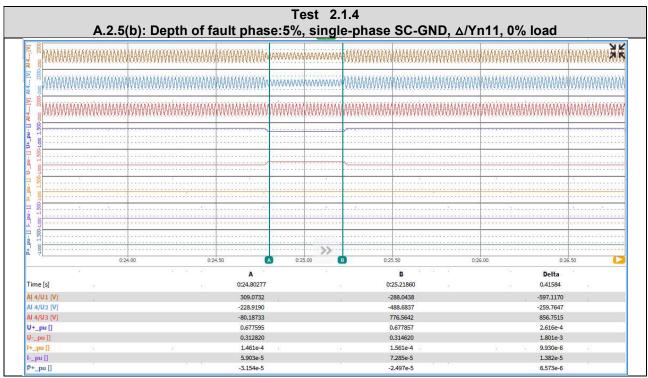
5.4.3(b)	5.4.3(b) LVRT Test (Load test - Δ/Yn11 transformer connection)							
Model: So	G3125HV-32					•		
Appendix	: Annex D (L	oad test)						
Test	Voltage Depth [pu]	Fault type	Fault duration [ms]	P set point [P _{rE}]	Set point [Ki]	P/F		
5.1.1		A 2 2 (b)	250	20%		Р		
5.1.2		A.2.2 (b)	250	100%		Р		
5.1.3		A.2.3 (b)	250	20%		Р		
5.1.4	0.05	A.2.3 (b)	230	100%	2	Р		
5.1.5	0.05	A.2.4 (b)	250	20%	2	Р		
5.1.6		A.2.4 (b)	250	100%		Р		
5.1.7		A 2 5 (b)	250	20%		Р		
5.1.8		A.2.5 (b)	250	100%		Р		
5.2.1		A 2 2 (b)	770	20%		Р		
5.2.2		A.2.2 (b)	770	100%		Р		
5.2.3	0.20	A.2.3 (b)	770	20%		Р		
5.2.4		0.20	A.2.3 (b)	770	100%	2	Р	
5.2.5		0.20	A.2.4 (b)	770	20%	7	Р	
5.2.6		A.2.4 (b)	110	100%		Р		
5.2.7		A.2.5 (b)	770	20%		Р		
5.2.8		A.2.5 (b)	770	100%		Р		
5.3.1		A.2.2 (b)	1800	20%		Р		
5.3.2				A.2.2 (b)	1800	100%		Р
5.3.3		A.2.3 (b)	1800	20%		Р		
5.3.4	0.50	A.2.3 (b)	1800	100%	_ 2	Р		
5.3.5	0.50	A.2.4 (b)	1800	20%		Р		
5.3.6		A.Z.+ (b)	1000	100%		Р		
5.3.7		A.2.5 (b)	1800	20%		Р		
5.3.8		A.2.3 (b)	1000	100%		Р		
5.4.1		A.2.2 b	3000	20%		Р		
5.4.2		A.Z.Z b	3000	100%		Р		
5.4.3		A.2.3 b	3000	20%	_	Р		
5.4.4	0.85	7.2.5 0	3000	100%	_ 2	Р		
5.4.5	0.00	A.2.4 b	3000	20%		Р		
5.4.6		M.Z.4 U	3000	100%		Р		
5.4.7		A.2.5 b	3000	20%		Р		
5.4.8		7.2.3 0	3000	100%		Р		

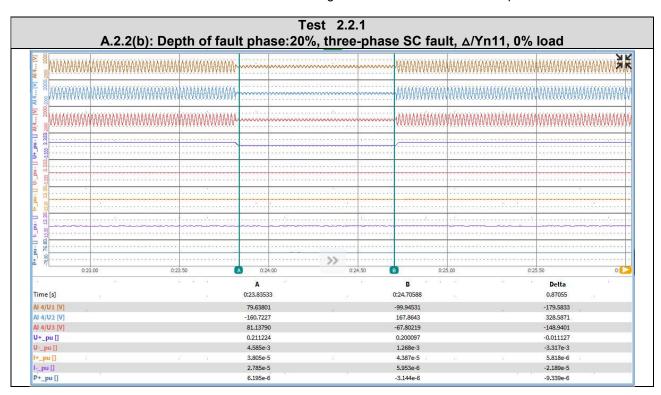
5.1(b)	LVRT Test (Δ		Р				
Model	SG3125HV-32						
	Required fault		Measu	red fault	Percentage of	Duration of	
Test number	Voltage pos. [pu]	Duration [ms]	Voltage pos. [pu]	Duration [ms]	current after fault [%lr]	restoring settling [ms]	
5.1.1			0.061	359	103	82	
5.1.2	0.05		0.053	338	104	243	
5.1.3			0.390	399	69.2	257	
5.1.4		250	0.389	385	67.0	298	
5.1.5	0.05	250	0.539	421	44.2	43	
5.1.6			0.539	394	46.1	267	
5.1.7			0.693	371	49.4	110	
5.1.8			0.693	371	50.5	277	
5.2.1			0.211	827	107	65	
5.2.2			0.231	834	108	272	
5.2.3	0.20		0.487	919	68.8	111	
5.2.4		770	0.486	923	66.0	306	
5.2.5			0.613	916	49.8	142	
5.2.6			0.611	912	49.6	247	
5.2.7			0.742	914	51.4	108	
5.2.8			0.742	905	51.6	292	
5.3.1			0.513	1880	103	140	
5.3.2			0.525	1912	100	237	
5.3.3			0.687	1910	64	135	
5.3.4	1	4050	0.689	1864	64	282	
5.3.5	0.50	1650	0.764	1873	49	145	
5.3.6			0.764	1870	49	255	
5.3.7			0.839	1834	30	105	
5.3.8			0.841	1810	31	130	
5.4.1			0.850	3022	29	215	
5.4.2			0.855	3080	31	145	
5.4.3			0.909	3045	19	175	
5.4.4	1 005	0000	0.912	3093	19	102	
5.4.5	0.85	3000	0.930	3028	14.1	178	
5.4.6			0.937	3057	14.2	122	
5.4.7			0.952	3088	10.1	156	
5.4.8	1		0.957	3082	10.1	114	

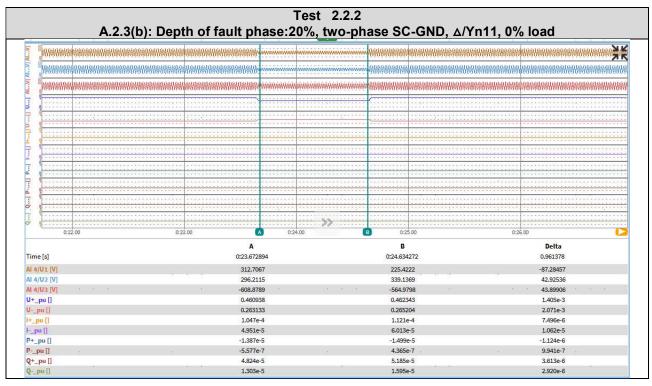


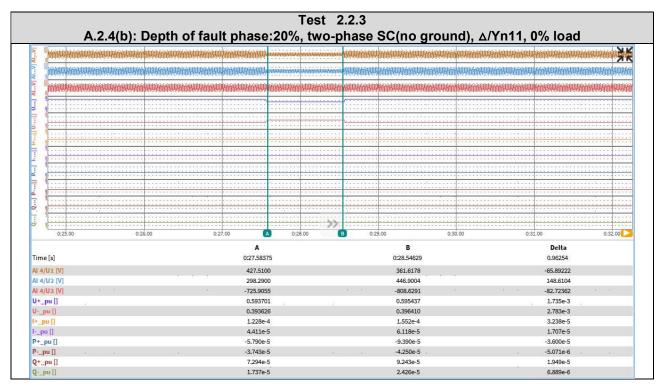


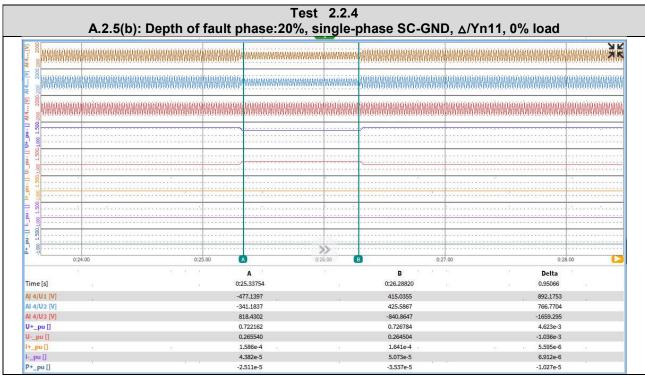


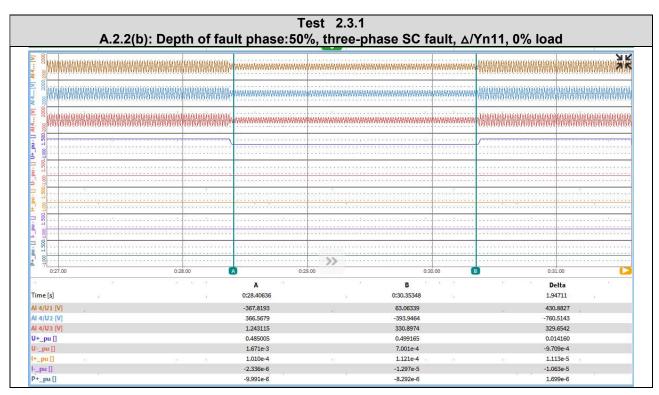


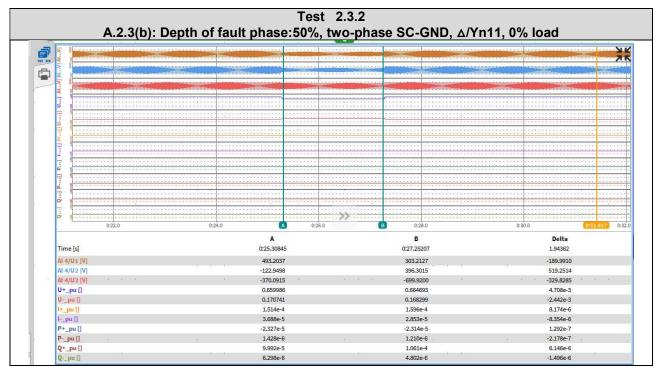


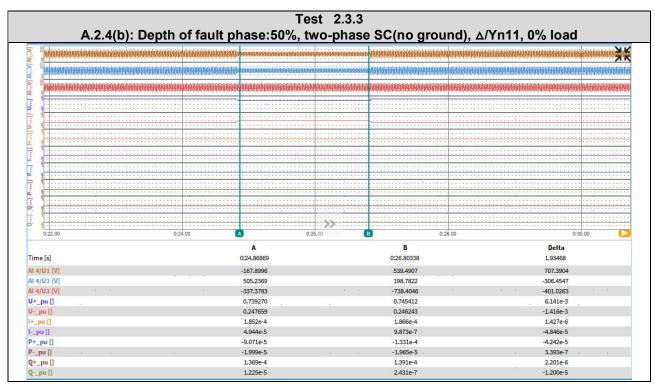


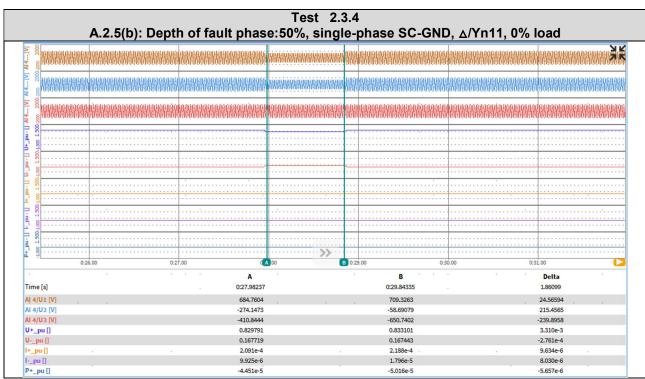


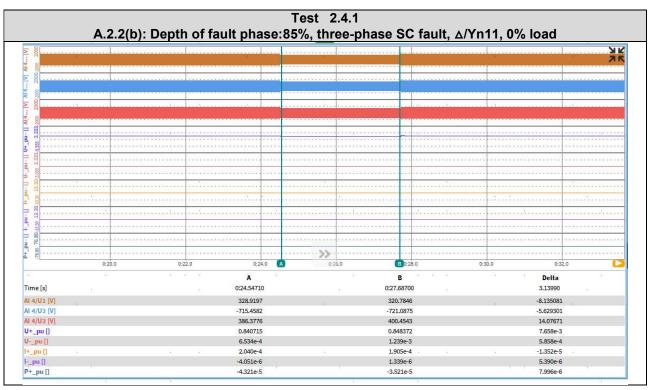


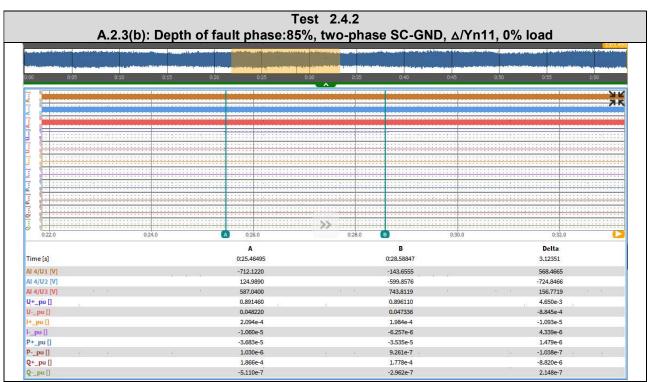


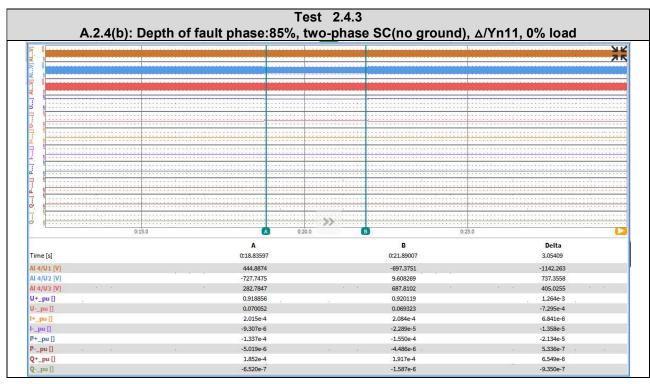


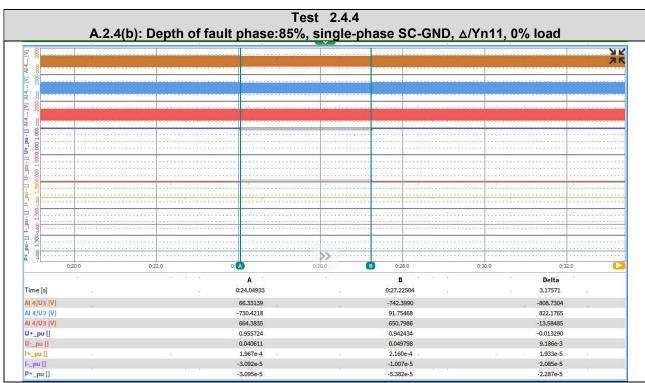


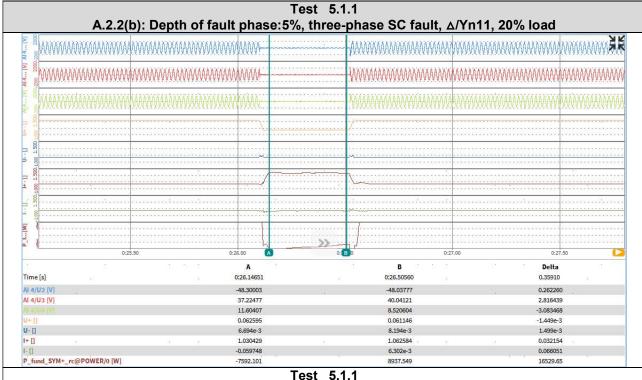




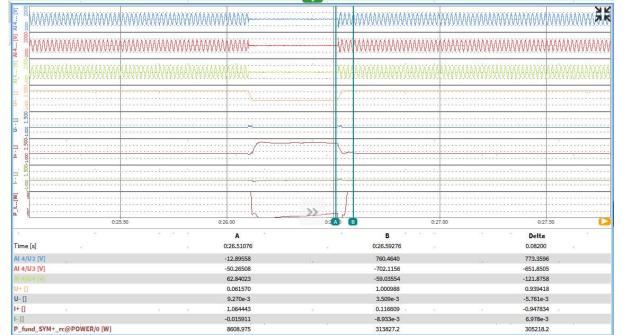






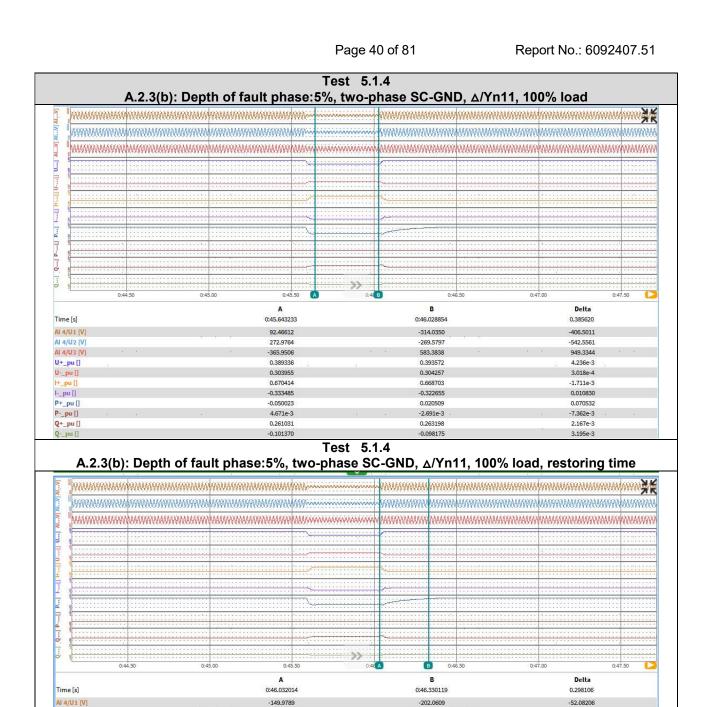


A.2.2(b): Depth of fault phase:5%, three-phase SC fault, △/Yn11, 20% load, restoring time









396,6401

0.394072

0.304803

0.670460

-0.324842

0.020265

-2.865e-3

0.264225

-0.099018

821.0204

1.000172

7.356e-3

8.578e-3

-2.210e-3

0.906418

1.070e-5

8 580e-3

-1.626e-5

424,3803

0.606100

-0.297448

-0.661882

0.322632

0.886153

2.876e-3

-0.255644

0.099002

Al 4/U3 [V]

U+_pu []

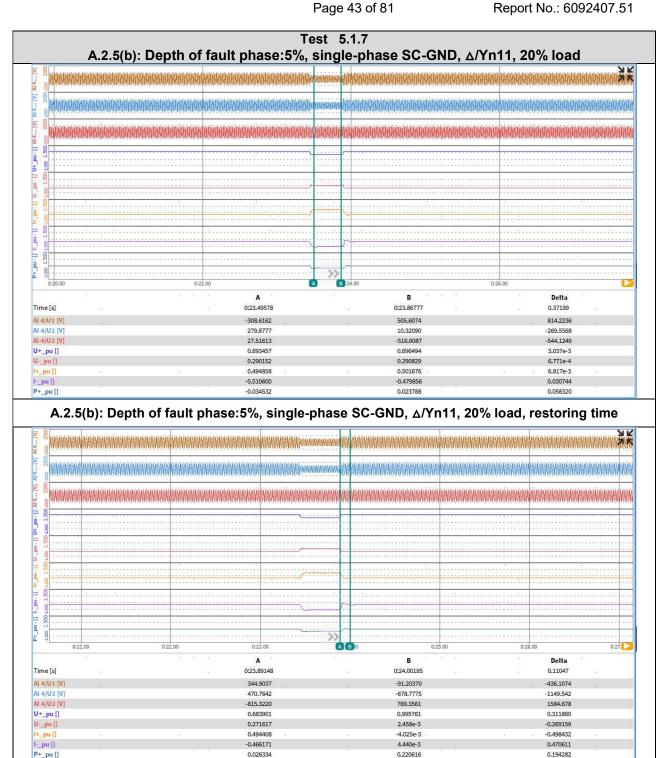
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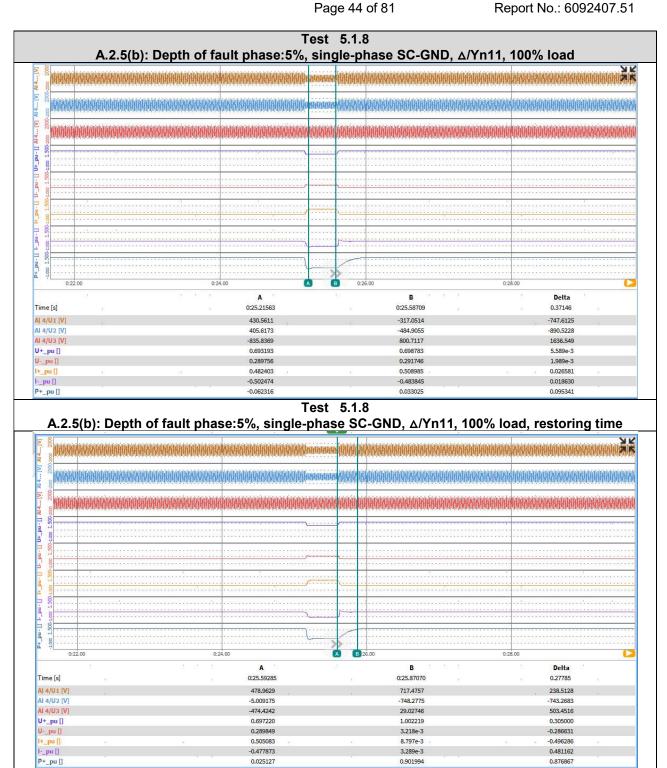
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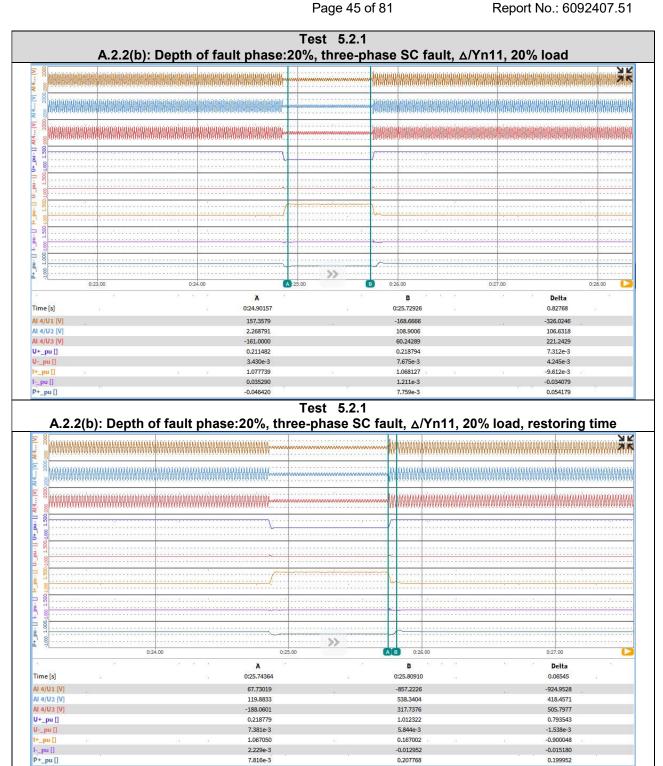
P+_pu [] P-_pu []



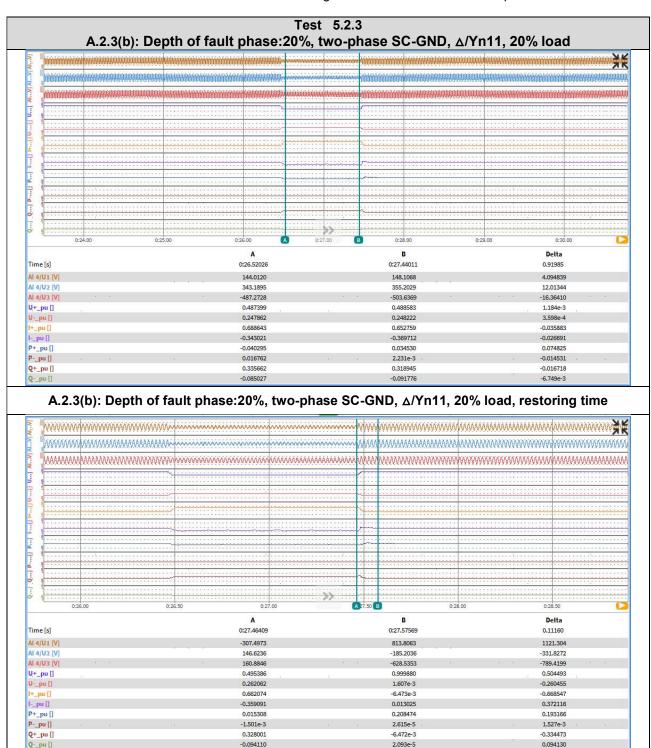




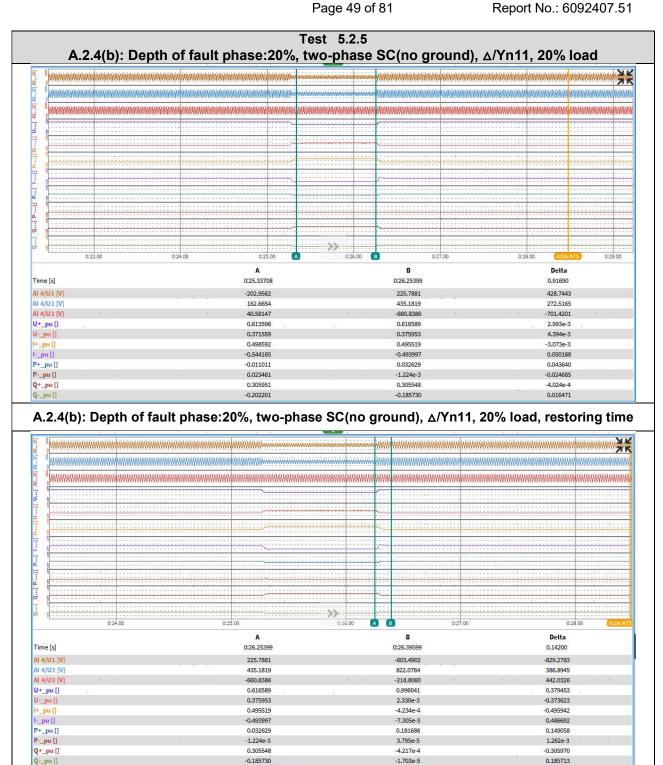


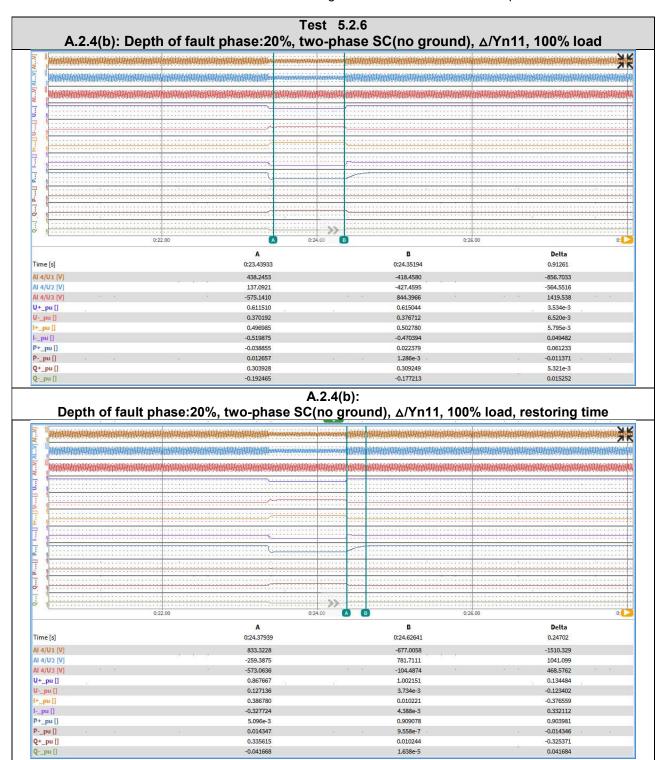




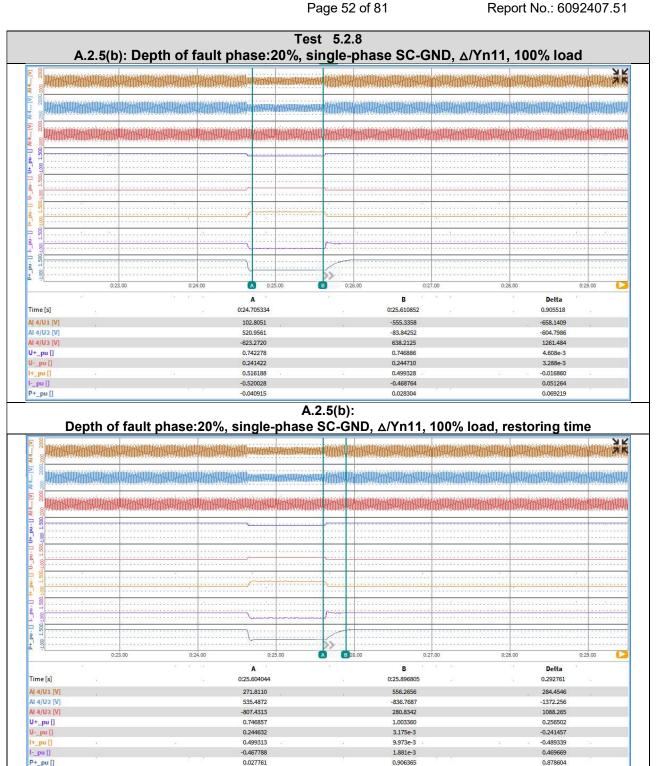






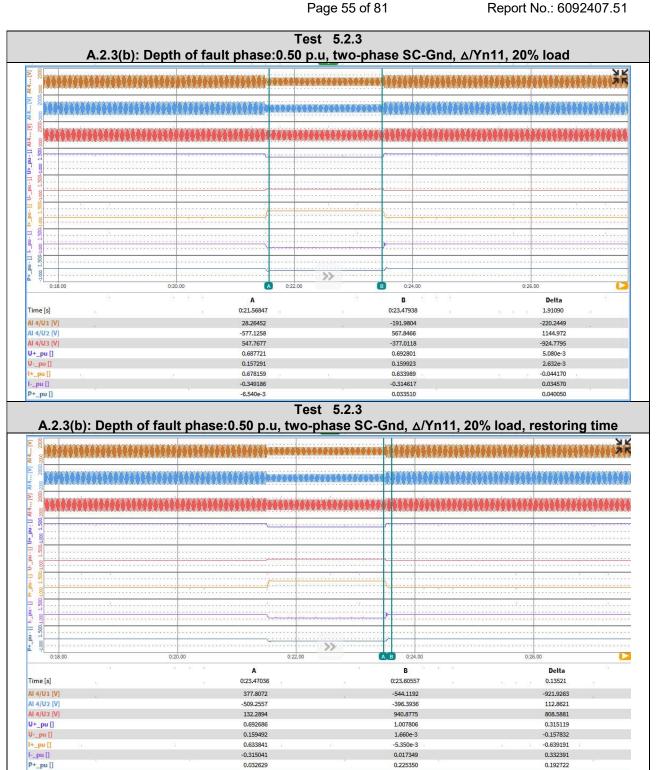








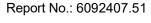


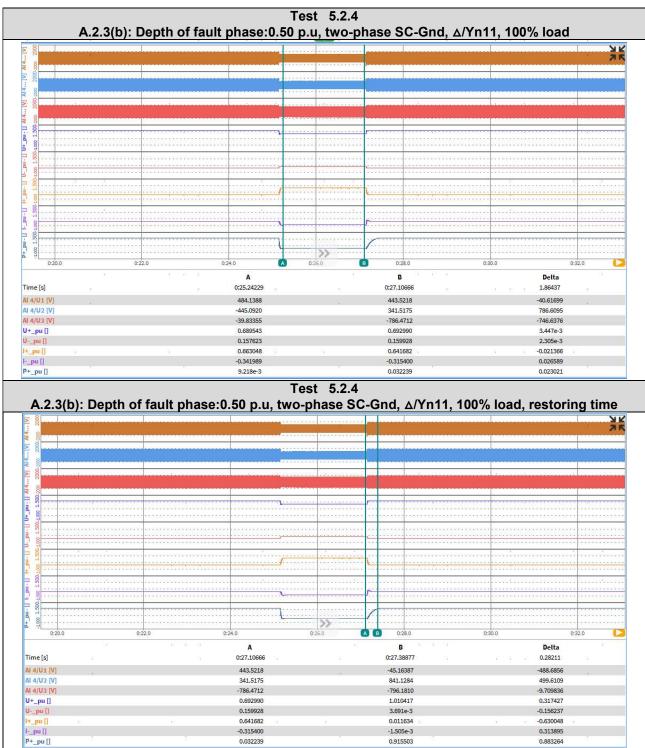


0.032629

0.225350

0.192722





Report No.: 6092407.51

-0.456892

0.041622

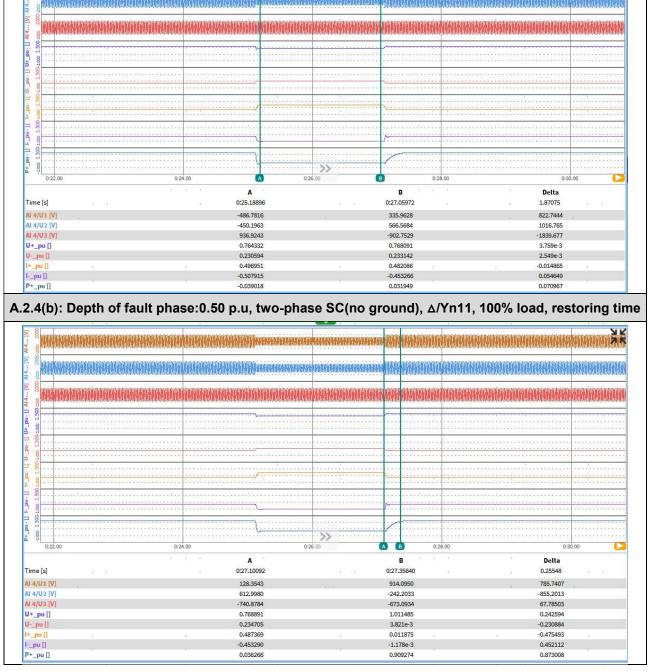
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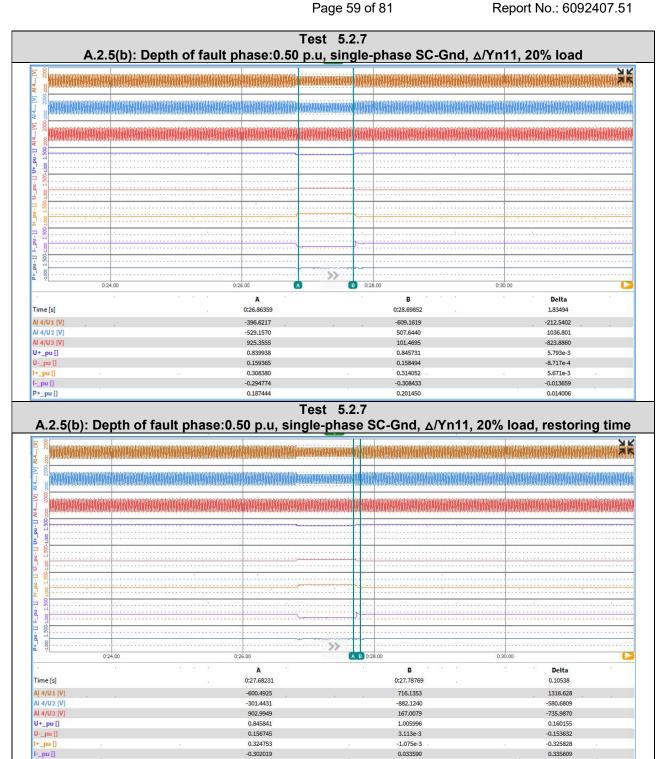
0.214930

0.463554

0.173308

I-_pu [] P+_pu []

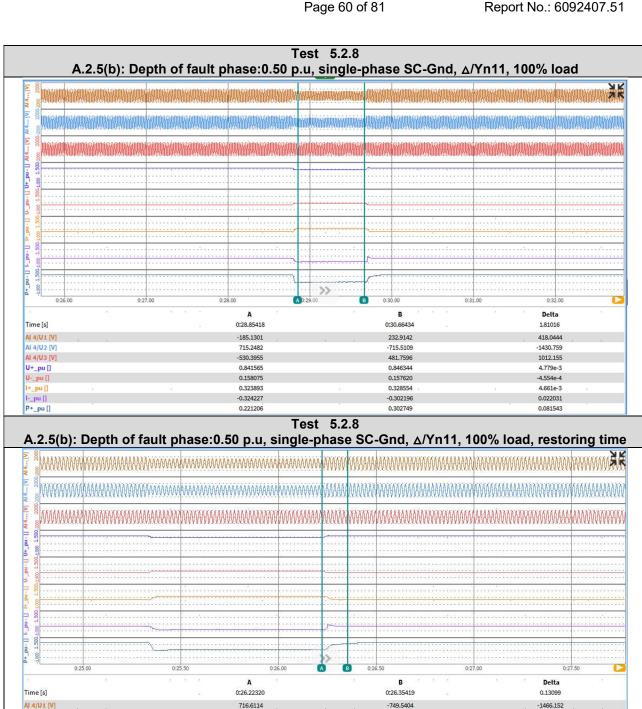




0.199781

0.200926

1.145e-3



-11.71756

-703.4657

0.846104

0.154872

0.315338

-0.302182

0.304161

-118.7310

867.8365

1.009260

3.756e-3

9.271e-3

9.975e-3

0.905193

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1571.302

0.163156

-0.151116

-0.306068

0.312157

0.601033

Al 4/U2 [V]

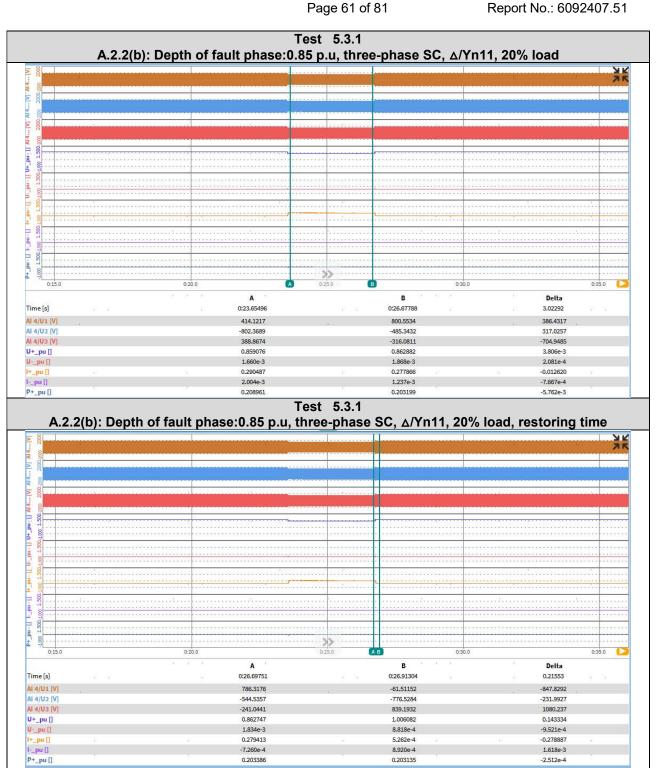
AI 4/U3 [V]

U+_pu []

U-_pu []

I-_pu []

P+_pu []





-77.77191

-700.8043

0.911845

0.049747

0.182074

-5.170e-3

0.202523

-934.5053

545.8699

1.005168

3.952e-4

-1.518e-3

-2.663e-4

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-0.183592

4.904e-3

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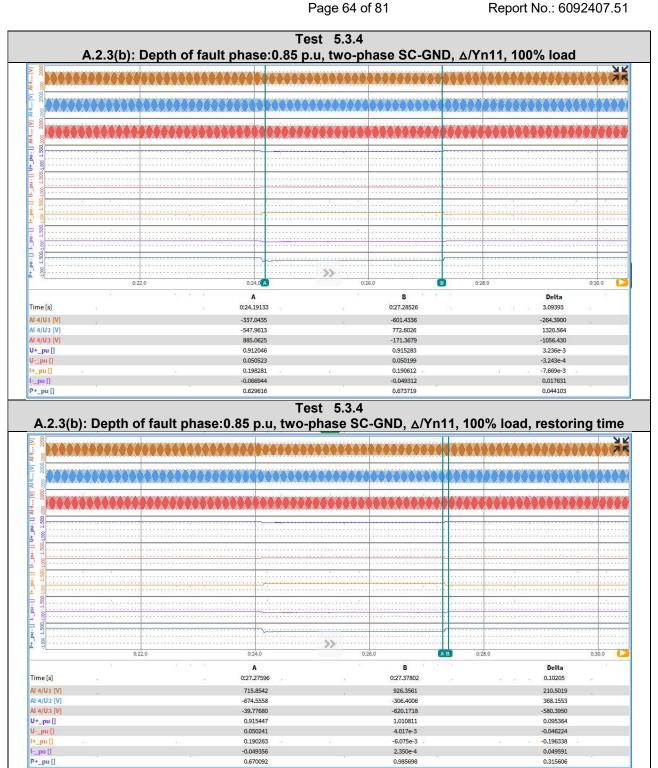
Al 4/U2 [V]

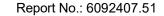
Al 4/U3 [V]

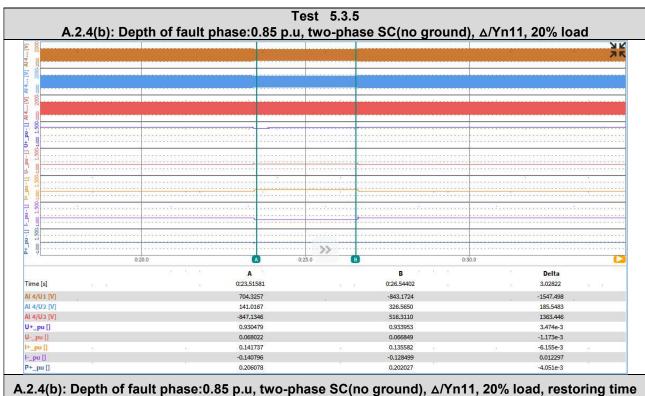
U-_pu []

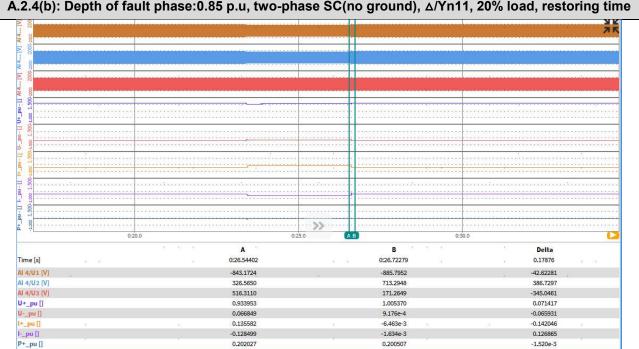
|+_pu [] |-_pu []

P+_pu []

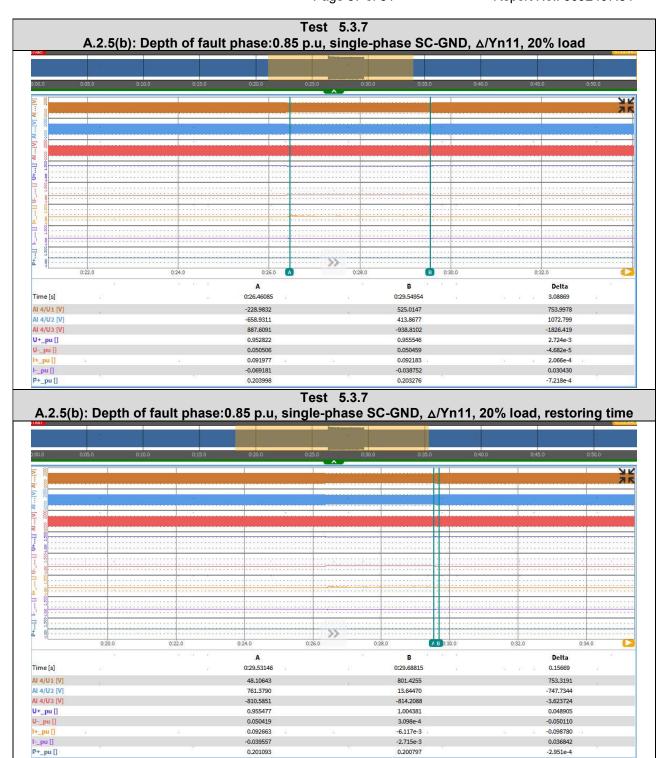


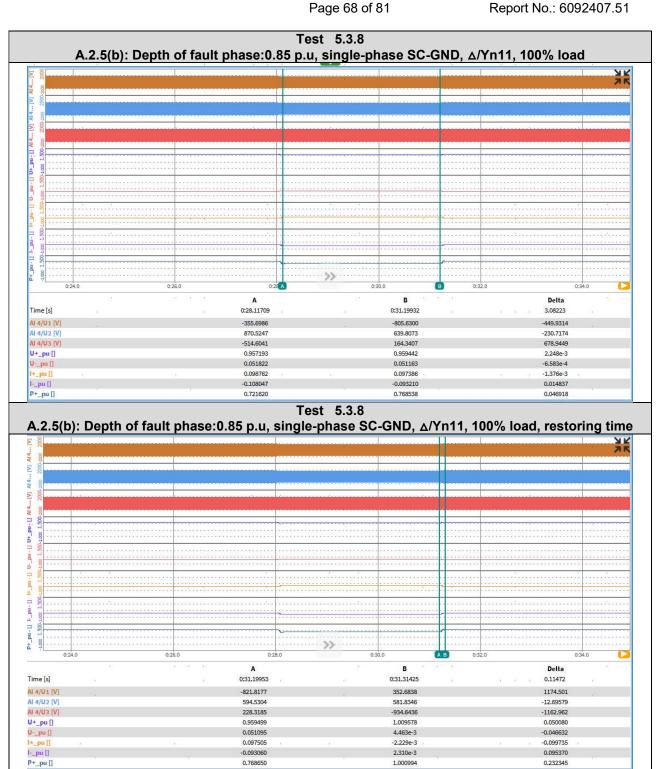




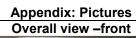








Report No.: 6092407.51



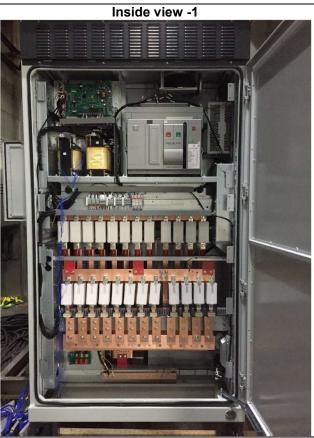


Overall view -back



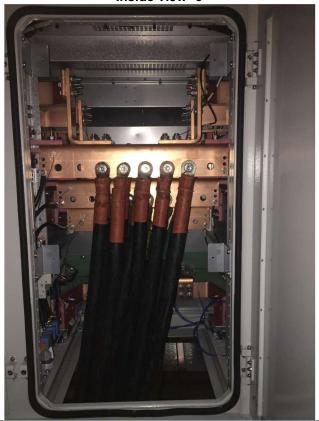












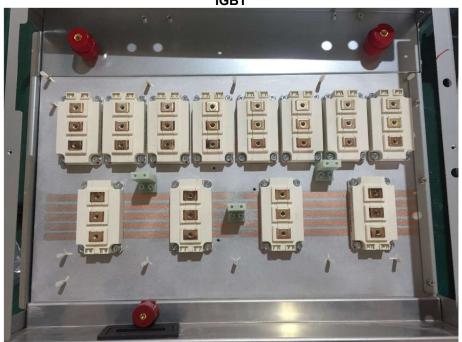
Isolating switch I

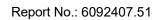




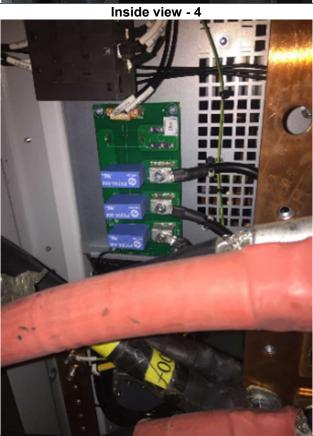


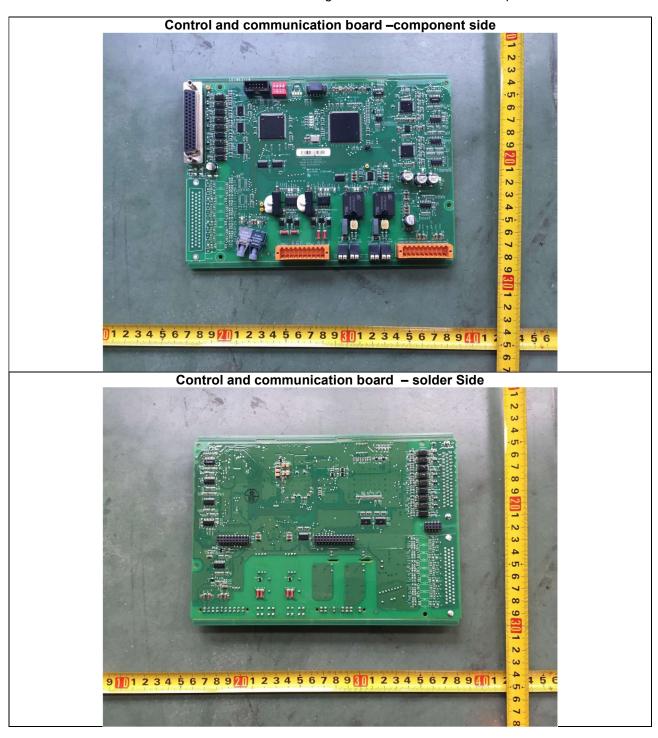


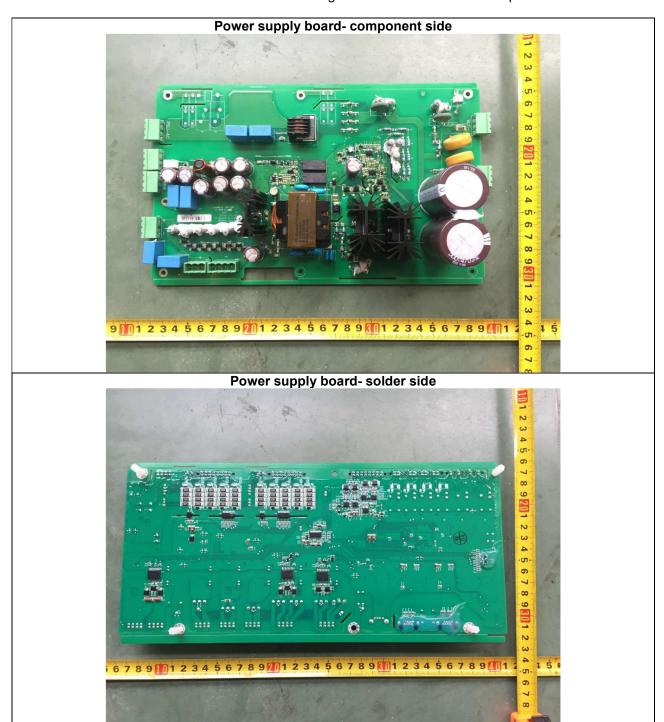


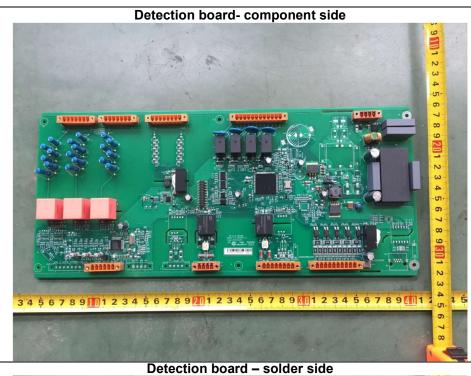


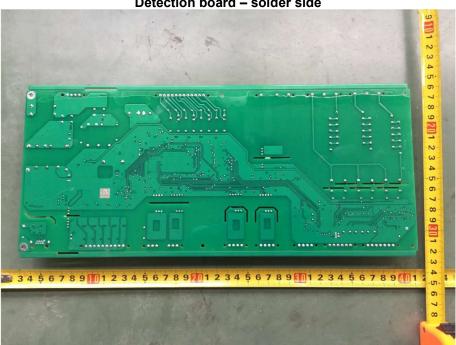


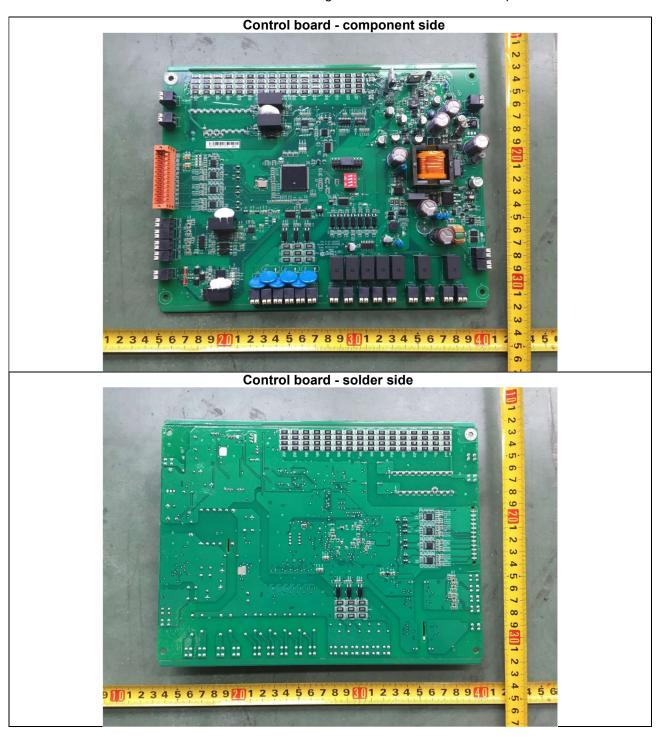


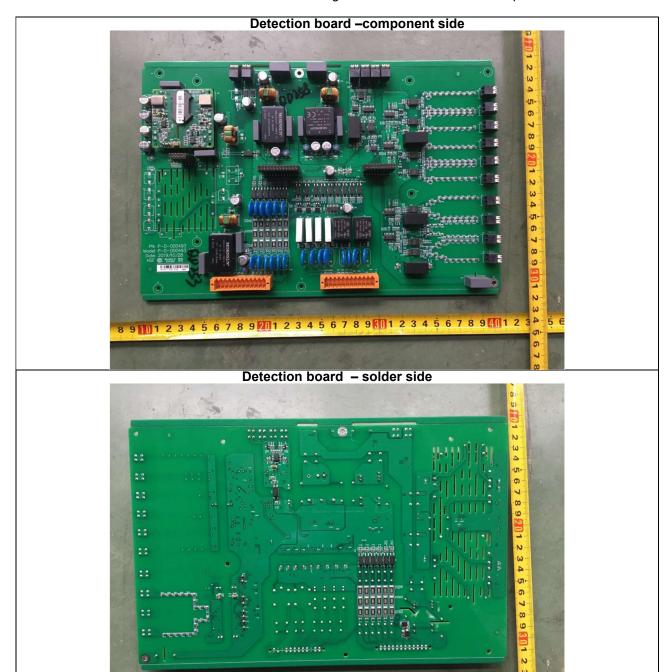




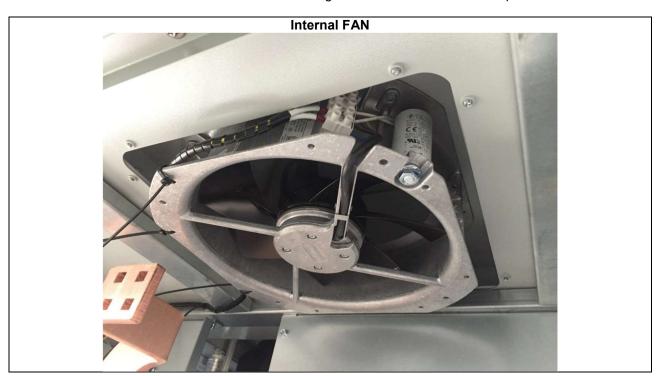








9 10 1 2 3 4 5 6 7 8 9 20 1 2 3 4 5 6 7 8 9 20 1 2 3 4 5 6 7 8 9 40 1 2



----- End of test report-----

ATTESTATION OF CONFORMITY

Issued to: Sungrow Power Supply Co., Ltd.

No.1699 Xiyou Rd., New & High Technology Industrial Development Zone,

230088, Hefei, P. R. China

For the product: Grid-connected PV inverter

旧 光 电 源 Trade name: SUNGROW

Type/Model: SG3125HV-30, SG3125HV-31, SG3125HV-32

Ratings: See Annex

Manufactured by: Sungrow Power Supply Co., Ltd.

No.1699 Xiyou Rd., New & High Technology Industrial Development Zone,

230088, Hefei, P. R. China

Requirements: IEC TS 62910:2020

This Attestation is granted on account of an examination by DEKRA, the results of which are laid down in a confidential file no. 6092407.51

The examination has been carried out on one single specimen or several specimens of the product, submitted by the manufacturer. The Attestation does not include an assessment of the manufacturer's production. Conformity of his production with the specimen tested by DEKRA is not the responsibility of DEKRA.

Arnhem, 23 December 2020 /// Number: 6092407,02AOC

DEKRA Testing and Certification (Shanghai) Ltd.

Kreny Lin Certification Manager

© Integral publication of this attestation and adjoining reports is allowed

Page 1 of 2

Kreny lin

Annex to 6092407.02AOC

Ratings of the test product:

Operating temperature range: - 35°C to + 60°C

Protective class: I

Ingress protection rating: IP65 (Optional IP55)

Power factor range (adjustable): 0.8 leading...0.8 lagging

SG3125HV-30:

PV input: Max. 1500 Vdc, MPPT voltage range: 875-1300 Vdc, max current: 3997 A, Isc PV: 10000 A Output: 600V, 3~, 50/60 Hz, max 3308 A, rated 3125 kW, max 3437 kVA

SG3125HV-31:

PV input: Max. 1500 Vdc, MPPT voltage range: 915-1300 Vdc, max current: 3997 A, Isc PV: 10000 A Output: 630V, 3~, 50/60 Hz, max 3308 A, rated 3125 kW, max 3610 kVA

SG3125HV-32:

PV input: Max. 1500 Vdc, MPPT voltage range: 960-1300 Vdc, max current: 3997 A, Isc PV: 10000 A Output: 660V, 3~, 50/60 Hz, max 3308 A, rated 3125 kW, max 3781 kVA